INNOVATIVE FPGA CONTROLLER CARD FOR INVERTER SYSTEMS

DISSERTATION PHASE - II REPORT

Submitted by

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Reg. No: MAC23ECVE05

to

APJ Abdul Kalam Technological University

In partial fulfilment of the requirements for the award of the Degree of

MASTER OF TECHNOLOGY

IN

VLSI AND EMBEDDED SYSTEMS

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MAR ATHANASIUS COLLEGE OF ENGINEERING

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MAY 2025

DECLARATION

I Mohammed Shehzad K Salim hereby declare that the Dissertation Phase II report "Innovative FPGA Controller Card For Inverter Systems",submitted for partial fulfilment of the requirements for the award of the degree of Master of Technology of the APJ Abdul Kalam Technological University, Kerala is a bonafide work done by me under supervision of Dr.Mathew K and Prof.Mary Joseph. This submission represents my ideas in my own words, and where ideas of others have been included, I have adequately and accurately cited and referenced the original sources. I also declare that I have adhered to the academic honesty and integrity ethics and have not misrepresented or fabricated any data, idea, fact, or source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the institute and/or the university and can also evoke penal action from the sources that have thus not been properly cited or from whom proper permission has not been obtained. This report has not previously formed the basis for the award of any degree, diploma, or similar title of any other university.

Place: Kothamangalam

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CERTIFICATE

This is to certify that the Dissertation Phase II report entitled **"Innovative FPGA Controller For Inverter Systems"** submitted by **Mohammed Shehzad K Salim** to the APJ Abdul Kalam Technological University in partial fulfillment of the requirements for the award of the Degree of Master of Technology in the Department of Electronics and Communication is a bonafide record of the project carried out by him under my/our guidance and supervision. This report in any form has not been submitted to any other University or Institute for any purpose.

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ACKNOWLEDGEMENT

First and foremost, I sincerely thank the 'God Almighty' for his grace for the successful and timely completion of the project.

I take this opportunity to express my deepest sense of gratitude and sincere thanks to everyone who helped me to complete this work successfully.I express my sincere gratitude and thanks to **Dr. Bos Mathew Jos** , our Principal, **Dr. Aji Joy**, Head of Department, **Prof. Mary Joseph** and **Prof. Nithin James** , Project Coordinators Electronics and Communication Engineering, Mar Athanasius College of Engineering, Kothamangalam for providing me with all the necessary facilities and support.

I would like to place on record my sincere gratitude to my project guide **Dr. Mathew K** , Professor, Electronics and Communication Engineering, Mar Athanasius College of Engineering for the guidance and mentorship throughout the course.

I express my sincere thanks to all the staff members in the Department of Electronics and Communication Engineering who have made sincere efforts to help me to complete this dissertation project

Finally I thank my family, and friends who contributed to the successful fulfilment of this project work.

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ABSTRACT

This dissertation presents the Phase II development of an FPGA-based controller for inverter systems that uses a two-level inverter topology. The controller leverages Sinusoidal Pulse Width Modulation (SPWM) to generate high-quality three-phase sinusoidal waveforms, ensuring efficient and reliable operation under varying load conditions. The hardware implementation, executed on the T20Q144I4 FPGA, successfully validates the SPWM output using an RC low-pass filter, which converts high-frequency switching signals into smooth sinusoidal waveforms. The proposed system demonstrates robust performance, maintaining stability under unbalanced load conditions 100% with minimal voltage regulation deviations. Furthermore, harmonic management techniques, including harmonic reduction and injection, ensure minimal Total Harmonic Distortion (THD). The controller supports variable output frequencies ranging from 40 Hz to 400 Hz and adjustable carrier frequencies, making it adaptable for diverse applications. Using the flexibility and processing speed of FPGA technology, the controller enables real-time adjustments and delivers optimal performance. The simplified two-level inverter architecture ensures ease of implementation while providing reliable power conversion. Phase 2 accomplishments establish a strong foundation for future developments, including advanced harmonic management, load optimization, and comprehensive operational enhancements, to achieve a versatile and efficient inverter control solution.

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1 INTRODUCTION

Building upon the foundational work established in Phase 1 of this dissertation, which successfully demonstrated the generation and validation of Sinusoidal Pulse Width Modulation (SPWM) signals using the T20Q144I4 FPGA, Phase 2 marks a critical transition towards the practical implementation of a complete FPGA-based inverter system. This phase is dedicated to the design and development of a printed circuit board (PCB) for a three-phase inverter with a 1kW load capacity, serving as a comprehensive platform for testing the FPGA controller card developed in the previous phase.

The shift from pure signal generation to a fully functional power electronics system introduces several engineering challenges. These include the need for effective thermal management, the mitigation of electromagnetic interference (EMI), the careful layout and routing of components, and the integration of robust protection mechanisms. Such considerations are essential to ensure reliable operation under varying load conditions and to protect both the power electronics and control circuitry from potential faults.

While Phase 1 validated SPWM signal generation using an RC low-pass filter and simulation tools such as LTSpice, MATLAB, and GTKWave, Phase 2 enables real-world testing with actual power flow and dynamic load conditions. This progression from signal validation to power validation represents a crucial step in the development of efficient and reliable AC inverter systems. The PCB design incorporates modern power semiconductor devices, isolated gate drivers, feedback sensing circuitry, protection mechanisms for fault detection and management, and interface circuits to connect with the FPGA controller card. The hardware architecture is designed for modularity and flexibility, allowing future enhancements and modifications as research advances.

In its current initial testing phase, the three-phase inverter PCB provides a platform to evaluate the performance of the FPGA controller under realistic operating conditions. Initial tests focus on verifying basic functionality, including proper power flow, successful transmission of the SPWM signal from the FPGA to the gate drivers, and the correct operation of the detection and protection circuits. This phase addresses the practical challenges of bridging the gap between theoretical control algorithms and their hardware implementation. The insights gained from the PCB design and testing process contribute valuable knowledge to the field of power electronics, particularly in the context of FPGA-based control systems for modern inverter applications.

2 LITERATURE REVIEW

2.1 Paper 1 : FPGA Implementation of Multiple Single Phase PWM Inverters with Configurable Duty Cycle and Dead Time

The survey discusses how FPGAs offer speed, flexibility, and reconfiguration compared to traditional microcontroller-based systems. This understanding is crucial in justifying the choice of FPGA for my project, particularly because of the parallel processing capabilities and high-speed operation that are vital for real-time control of inverters. The flexibility to reconfigure control algorithms in an FPGA aligns well with my project's requirements for multiple single-phase PWM inverters with configurable duty cycles and dead time.

The survey outlines the use of Sinusoidal Pulse Width Modulation (SPWM) as an effective method of controlling inverter switches while reducing harmonic distortion. Studies by Bakar et al. and Annapoorani et al. demonstrate how SPWM can be efficiently implemented on FPGAs using VHDL or Verilog, providing a strong foundation for the FPGA-based SPWM control system in my project. The literature survey strongly advocates for FPGAs as a preferred platform due to their parallel processing, reconfiguration, and high-speed operation. These features are directly relevant to my project, which involves multiple PWM inverters with configurable control strategies.

The literature survey from the base paper provides a strong foundation for my project, particularly in its focus on FPGA-based control for inverters. Key insights into SPWM implementation, reconfiguration, and real-time control have directly influenced my design choices for implementing multiple single-phase PWM inverters with configurable duty cycle and dead time. The survey justifies the use of FPGAs over traditional microcontrollers due to their superior performance in handling complex control tasks with high speed and flexibility. Using the lessons learned from previous works, we can confidently design a system that is scalable, adaptable, and capable of delivering high-quality power conversion with reduced harmonics and optimized switching.

2.2 Paper 2 : Implementation of FPGA-Based MSPWM Using 6-Input LUT for Reference Signal Generation

The introduction of the supporting paper highlights the growing adoption of FPGAs in inverter systems due to their flexibility, high-speed operation, and ability to handle parallel

processing. These attributes are particularly relevant to my project, which requires the ability to control multiple single-phase inverters with independent and configurable parameters such as duty cycle and dead time.

The primary contribution of the supporting paper is the discussion on the use of 6-input LUTs for the generation of the SPWM reference signal. This LUT-based approach significantly reduces the usage of resources in the FPGA, which is critical for implementing a system that controls multiple inverters while maintaining efficiency in resource allocation.

The paper presents the innovative use of 6-input LUTs to generate high-resolution SPWM reference signals with minimal resource consumption. This LUT optimization is a crucial strategy in my project, where multiple single-phase inverters are controlled, and the efficient use of FPGA resources is essential. The paper, "FPGA-Based Implementation of MSPWM Using 6-Input LUT for Reference Signal Generation" has directly contributed to the development of my project in several ways.

- Efficient SPWM Generation Using LUTs: The use of 6-input LUTs to generate SPWM signals with reduced resource consumption is a key contribution. By adopting this approach, my project can efficiently manage the FPGA resources while implementing configurable duty cycles and dead time for multiple inverters.

- Real-Time and High-Speed FPGA Operation:The high-speed operation of FPGAs, as discussed in the paper, enables real-time control of multiple inverters, ensuring precise switching and efficient power conversion in my design.

- Resource Optimization: The resource optimization strategies outlined in the paper are essential for handling the multiple tasks involved in controlling multiple inverters. By reducing the size of the LUTs and efficiently managing FPGA resources, my project can maintain scalability and flexibility.

- Overcoming Implementation Challenges: The paper addresses key challenges such as managing precision and resource trade-offs, providing solutions that my system can apply to ensure the accuracy and performance of my system without exceeding the available FPGA resources.

In summary, the literature survey in the supporting document has significantly influenced the approach of my project to SPWM generation, resource optimization, and real-time control,

all of which are critical for the successful implementation of multiple single-phase PWM inverters.

2.3 Paper 3 : Implementation in FPGA of an Alternative Modulation Strategy for Energy Balancing Purposes

The supporting article highlights the increasing role of FPGA-based control systems in inverter applications, particularly in high-power, grid-connected, and renewable energy systems. These applications demand real-time control, flexibility, and energy balancing, making FPGAs the ideal platform for implementing advanced modulation strategies. The paper underscores the importance of using FPGAs to optimize switching patterns for efficient energy distribution, which is also a core aspect of my project. The paper discusses multiple PWM techniques, including phase-shift PWM (PS-PWM) and level-shift PWM (LS-PWM), which are particularly useful in multilevel inverters. However, these PWM techniques also offer insight into the management of power distribution and harmonic distortion, which are critical in my single-phase PWM inverter project.

The core focus of the supporting paper is the implementation of an alternative modulation strategy based on FPGAs aimed at energy balance in multilevel inverters. The paper demonstrates how FPGAs are used to manage complex switching algorithms and energy balancing through advanced modulation strategies. This is directly applicable to my project, where managing configurable duty cycles and dead time involves complex real-time adjustments that FPGAs are well suited to handle.

The paper emphasizes the need for energy balancing in multilevel inverters to ensure reliable operation, reduce system losses, and extend the lifetime of inverter components. The supporting paper provides a detailed comparison of harmonic distortion in various PWM techniques, which is critical in ensuring high power quality in grid-connected inverter systems. In my project, ensuring low THD and high power quality is essential, especially when controlling multiple inverters simultaneously.

The supporting document highlights the advantages of using FPGAs to implement advanced modulation strategies in inverter control systems, particularly for energy balance and harmonic performance. These insights are directly relevant to my project, where FPGAs enable flexible and high-speed control over multiple inverters with configurable duty cycles and dead time.

3 METHODOLOGY

The development of a 1kW three-phase inverter with multifrequency capability marks a notable step forward in the versatility of power electronics. This system finds applications in industrial motor drives, aerospace power systems, and frequency conversion equipment. My design brings together several carefully engineered power processing stages to deliver reliable three-phase AC output at user-selectable frequencies of 50Hz and 60Hz. The approach I have taken includes DC-AC conversion, step-up voltage transformation, and robust protection mechanisms that meet industrial standards. My system operates from a regulated 320V DC

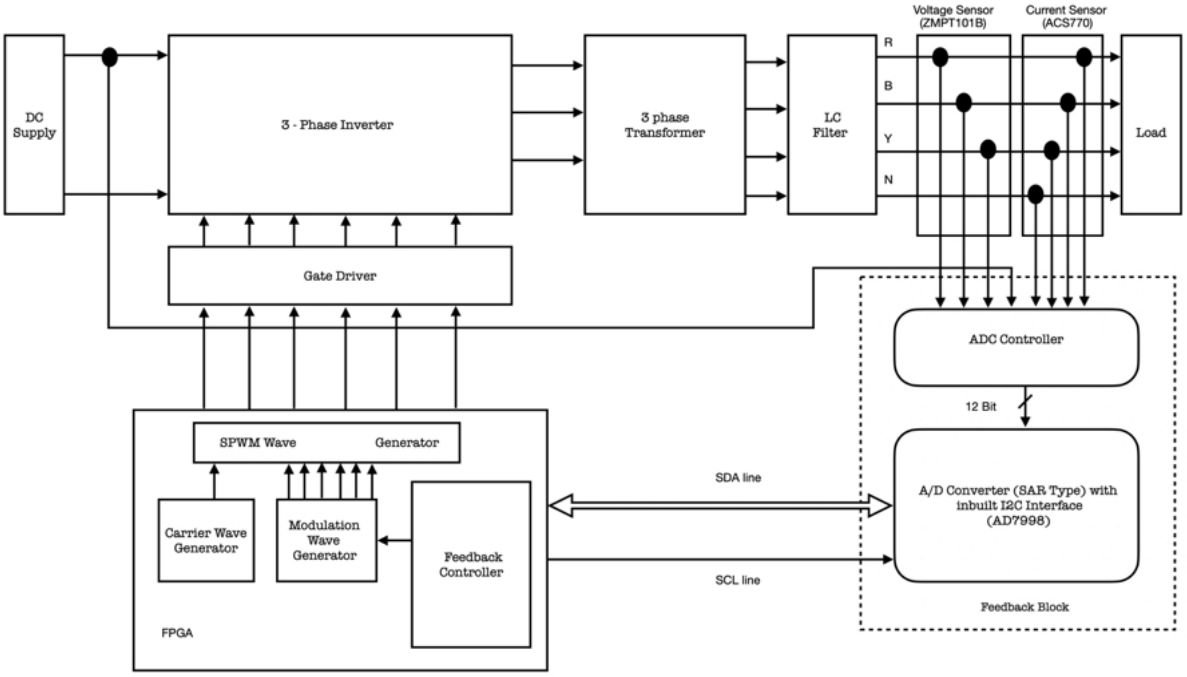


Figure 3.1: The Proposed System

bus that serves as the primary power source. This DC input undergoes conversion through a six-switch IGBT-based three-phase bridge using Infineon IKP40N65H5XKSA1 power transistors rated at 650V/40A. I specifically selected these components for their generous 4.16× peak current margin and 2× voltage headroom, which helps ensure dependable operation even when load conditions vary. These IGBTs switch at 20kHz to generate three-phase AC waveforms on the primary side with minimal distortion. For gate drive signals, I have implemented isolated TI UCC21520DW drivers that provide 5kVRMS isolation and 150V / ns common mode transient immunity - features I found essential for rejecting noise in environments with rapid voltage transitions. The generated AC signals pass through the EE-55 transformer. The EE-55

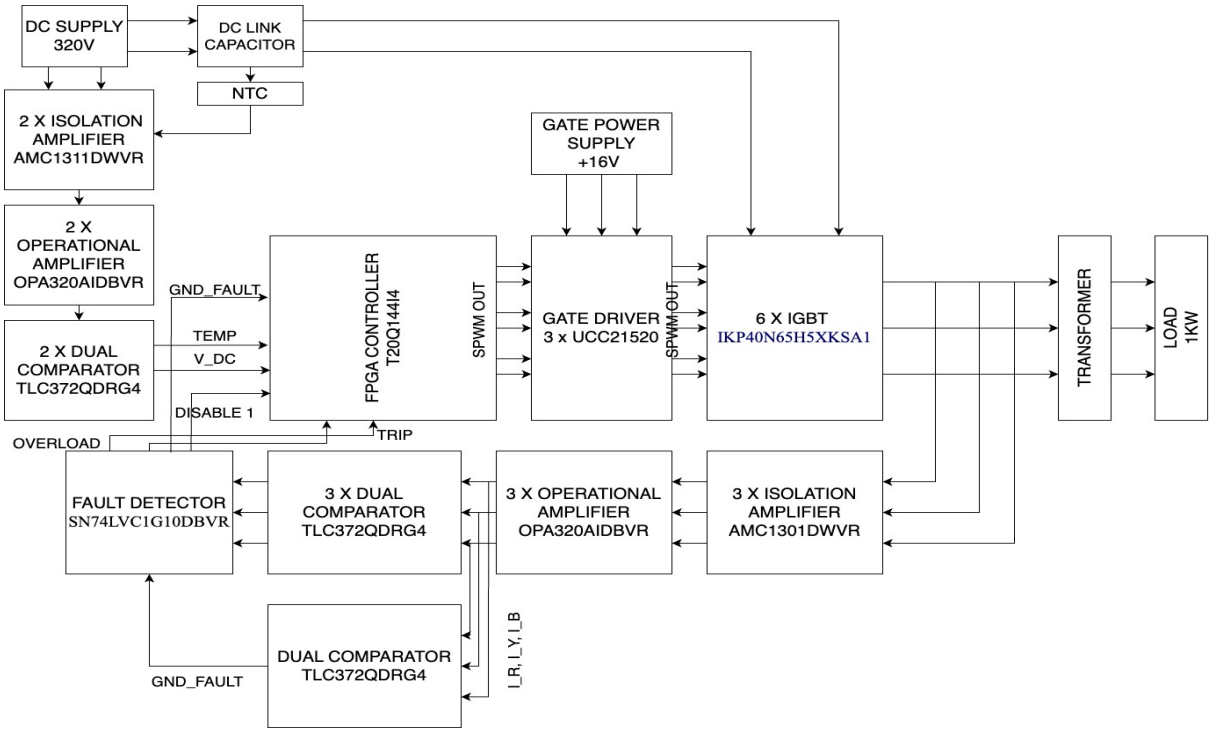


Figure 3.2: The Proposed Inverter Design

transformer handles the voltage conversion from 101.8V to 400V. I chose the EE-55 core configuration after careful consideration of several factors, including power handling capability, core loss characteristics, and manufacturing practicality. The EE core structure offers a good balance between winding ease and magnetic efficiency, with the added benefit of being more readily available and cost-effective than specialized core types.

For system protection, I have implemented a multilayered approach that combines basic and advanced safety mechanisms. This strategy ensures long-term reliability and rapid response to fault conditions. The thermal management system I designed uses appropriately sized heatsinks. Temperature monitoring is handled by strategically placed NTC thermistors that continuously check operating temperatures, ensuring that they remain well below the 175 $^{\circ}$ C maximum rating of the IKP40N65H5XKSA1 IGBTs even under full load.

I paid particular attention to electromagnetic compatibility in this design. The 4-layer PCB implementation features dedicated ground and power planes that significantly reduce loop inductance and common-mode emissions. The EE-55 transformers, while not offering quite the same inherent EMI advantages as toroidal types, are complemented by carefully designed filtering components to maintain CISPR 22 Class A compliance. The FPGA-based control system that I developed provides precise timing for dead-time insertion, frequency selection between 50Hz and 60Hz, and coordinated response to fault conditions.

My methodology delivers a robust platform for frequency-flexible power conversion while meeting industrial standards, including IEC 61800-5-1 and IEC 60664-1. The three independent EE-55 transformers enhance phase balance and isolation, which I found crucial to delivering high-quality three-phase power. The combination of IKP40N65H5XKSA1 IGBT and UCC21520DW gate drivers ensures excellent switching performance at 20kHz, with sufficient headroom for reliable operation under various thermal and electrical stress conditions. The EE-55 transformer configuration adapts well to multiple frequencies, and when paired with the protection mechanisms and thermal management systems I have implemented, ensures dependable operation across diverse environmental conditions and load profiles.

Through extensive testing and refinement, I have created a system that balances performance, reliability, and cost-effectiveness for applications that require precise frequency control and stable three-phase output power.

4 DESIGN ASPECTS

The design and implementation of a three-phase Voltage Source Inverter (VSI) using EE55 transformers encompass multiple critical stages. Each phase of the process is integral to achieving a robust, efficient, and reliable system capable of meeting the demands of various applications. Below is an exploration of the key design aspects as detailed in the project.

1. Topology Selection : The first step in designing the three-phase VSI involves selecting the appropriate topology. This decision is influenced by several factors, such as the required power rating, efficiency considerations, and the specific application for which the inverter is intended. For this 1kW design, a three-phase bridge topology with EE55 ferrite transformers was selected. Based on the search results, the EE55 transformers can handle between 1000W-1500W of power, making them suitable for this application. The EE55 core structure offers excellent power handling capability while maintaining reasonable size constraints. This topology supports operation at 50Hz and 60Hz frequencies, providing versatility for various regional power standards while maintaining good efficiency levels.

2. Component Selection : Once the topology is finalized, the next step focuses on the careful selection of electronic power components. The reliability and efficiency of the VSI depend heavily on the components used in its construction. For this design, Infineon IKP40N65H5XKSA1 IGBTs were selected for their superior switching characteristics, featuring 650V breakthrough voltage with a factor of 2.5 lower gate charge and factor 2 reduction in switching losses compared to previous generations. These IGBTs are optimized for switching frequencies from 30kHz to 100kHz, making them ideal for 20kHz operation in this inverter. The gate driver selection was centered on the UCC21520DW, which provides a 4A source and 6A sink peak current with reinforced isolation of 5.7kVRMS and a minimum of 125V/ns common-mode transient immunity. For the transformers, EE55 ferrite cores were chosen based on their working frequency range of 20kHz-500kHz and output power capability of 80-2000W, as indicated in the search results. EE55 transformers offer convenient winding characteristics, moderate pricing, and high reliability according to manufacturer specifications.

3. Circuit design : The design phase progresses with the creation of the circuit architecture for the VSI. This involves a detailed schematic design that incorporates key elements such as the configuration of the three-phase bridge with EE55 transformers. According to the search results, the EE55 transformers have a horizontal structure with dimensions of approximately 57.3mm×54.5mm×51.0mm, allowing for efficient PCB layout. The transformers can operate

at the required 20kHz switching frequency and handle the 1kW power requirement. Circuit protection includes both basic mechanisms (fuses with 10-20ms response time) and advanced features (desaturation detection with <1us response time). The layout incorporates a 4-layer PCB design with dedicated ground and power planes to minimize loop inductance and reduce common-mode emissions. The EE55 transformers, with their 16-20 pin configuration, as mentioned in the search results, provide sufficient connection points for complex winding arrangements needed in three-phase applications.

4. Central Controller Board : The design also includes the development of the Central Controller Board, which serves as the brain of the VSI. An FPGA-based control system is utilized as the central processing unit, providing precise timing for dead-time insertion, frequency selection (50Hz/60Hz), and synchronous response to fault conditions. The controller board emphasizes seamless integration with other components, including IGBTs IKP40N65H5XKSA1, UCC21520DW gate drivers, and sensing circuits. The UCC21520 gate drivers feature internal functional isolation between the two secondary-side drivers, allowing a working voltage of up to 1500VDC. Each driver can be configured for half-bridge operation with programmable dead-time, ensuring precise control over the switching sequences. A disable pin allows for emergency shutdown of both outputs simultaneously, with fail-safe measures forcing both outputs low in case of primary-side logic failures.

5. Control Algorithms: A critical aspect of the design is the development of control algorithms that dictate the operation of the inverter. These algorithms are designed to achieve specific performance objectives, such as maintaining voltage regulation, minimizing harmonic distortion, and ensuring fault tolerance. For the three-phase VSI, synchronously rotating reference frame control was implemented for its simplicity and effectiveness in grid-connected applications. The control system generates precise PWM signals at 20kHz with <100ns dead time to minimize distortion. Temperature monitoring via NTC thermistors maintains junction temperatures below the IKP40N65H5XKSA1 maximum rating of 175 ° C even under maximum load conditions. The FPGA implementation allows for adaptive control strategies that can respond to changing load conditions or adjust parameters based on the selected operating frequency (50Hz/60Hz), ensuring optimal performance across the full operating range. The operating temperature range of the EE55 transformers from -40 ° C to +125 ° C (as indicated in the search results) provides sufficient thermal headroom for reliable operation.

6. Testing and Optimization : After the design and implementation are completed, the

system undergoes rigorous testing and optimization. This phase ensures that the VSI meets the desired specifications and performs reliably under various operating conditions. Testing involves evaluating the system at different frequencies (50Hz and 60Hz) and load conditions to verify performance meets the efficiency targets. According to the search results, the EE55 transformers can operate efficiently within the -40°C to +85°C temperature range, which is verified during thermal testing. Parameters such as total harmonic distortion, EMI compliance, and thermal behavior are analyzed. Special attention is given to the transformer's performance at the 20kHz switching frequency, as the search results indicate that this is within the EE55's optimal working frequency range of 20kHz-500kHz. The testing confirms that the EE55 transformers can handle the required power levels of 1000W as specified in the search results for models like the 55EE-1111BNL, which is rated for 400VAC, 1000W output with 12VDC input at 100kHz.

The design of a three-phase VSI using EE55 transformers, IKP40N65H5XKSA1 IGBTs, and UCC21520DW gate drivers represents a comprehensive integration of advanced components for superior performance. The EE55 transformer configuration provides excellent power handling capability and frequency response, while the selected IGBTs and gate drivers ensure efficient switching performance optimized for 20kHz operation. By meticulously addressing these aspects, the design achieves good efficiency, EMI performance, and thermal management, making it suitable for a wide range of applications that require multi-frequency capability and high reliability.

4.1 Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal Pulse Width Modulation (SPWM) is a widely used technique in power electronics to convert DC power to an AC output with a sinusoidal waveform. This method is fundamental in inverters used for applications such as motor drives, renewable energy systems, and uninterruptible power supplies (UPS). By modulating the width of the pulses in a way that corresponds to a sine wave, SPWM ensures the generation of an AC output with reduced harmonic distortion and precise voltage regulation. Two common SPWM techniques, unipolar SPWM and bipolar SPWM, offer distinct advantages and trade-offs, making the selection process application specific.

4.1.1 Unipolar SPWM

Unipolar SPWM generates the output waveform by comparing a sinusoidal reference signal with two carrier signals that are 180 ° out of phase. This results in the output voltage switching between 0 and +Vdc or 0 and -Vdc, avoiding direct transitions between +Vdc and -Vdc. The staggered nature of the voltage transitions makes unipolar SPWM efficient and reduces harmonic distortion.

Advantages of Unipolar SPWM:

- **Lower Harmonic Distortion:** Dominant harmonics appear at twice the carrier frequency, making it easier to filter out unwanted components.
- **Reduced Electromagnetic Interference (EMI):** Smaller voltage transitions and reduced high-frequency content minimize EMI.
- **Lower Switching Losses:** Fewer and less frequent transitions between high voltage levels reduce power loss.

Despite these benefits, unipolar SPWM has a significant limitation: lower DC bus utilization. This means that the amplitude of the fundamental output voltage is reduced in comparison to the available DC voltage, making it unsuitable for applications that require the maximum output voltage.

4.1.2 Bipolar SPWM

Bipolar SPWM, on the other hand, compares a single sinusoidal reference signal with a single carrier signal. The output voltage switches directly between +Vdc and -Vdc, simplifying the implementation and ensuring better utilization of the DC bus.

- **Higher DC Bus Utilization:** Bipolar SPWM delivers a higher output voltage amplitude, maximizing the available DC input voltage.
- **Simpler Implementation:** The use of a single carrier signal and a straightforward comparison simplifies circuit design.
- **Robust Performance:** Bipolar SPWM is less affected by load imbalances and can maintain stable operation under varying conditions.

However, the higher voltage swings in bipolar SPWM result in increased switching losses and slightly higher harmonic distortion. These challenges can be addressed by employing efficient semiconductor devices (e.g., MOSFETs) and using filtering techniques such as RC or LC networks.

For this dissertation, bipolar SPWM was selected as the preferred modulation technique due to its superior DC bus utilization and straightforward implementation. These characteristics make it highly suitable for applications that require robust and high-quality power conversion. The following factors influenced this choice:

- **Higher Output Voltage:**Bipolar SPWM ensures the fundamental output voltage amplitude is closer to the DC input, which is essential for driving inductive loads such as motors.
- **Simpler Control:** The simpler logic of bipolar SPWM aligns well with FPGA-based implementations, minimizing resource utilization while achieving reliable performance.
- **Robust Operation Under Load Variations:** Bipolar SPWM demonstrates consistent performance even under unbalanced load conditions, which aligns with the project's focus on ensuring stability and efficiency.

4.2 H-Bridge Topology in SPWM Inverter Systems

The H-Bridge is a fundamental building block of inverter systems, especially in DC-AC converters. The H-Bridge circuit consists of four switches (transistors, MOSFETs, or IGBTs) arranged in an H-like configuration. By controlling which switches are turned on and off, the current direction across the load can be controlled, allowing for the generation of an AC waveform. In the H-Bridge, switching the diagonal pairs of switches on and off generates positive and negative voltage across the load, producing the necessary AC output. This architecture is crucial to achieve high efficiency in inverters. For three-phase inverter systems, multiple H-Bridge configurations are used to generate the three AC phases, each shifted by 120 degrees. The simplicity of the H-Bridge design makes it a highly reliable and widely adopted method for motor control and inverter applications.

The H bridge converter is a popular and versatile converter used in various applications. It consists of four IGBTs and four antiparallel diodes, with Ta+ and Tb- being the upper and

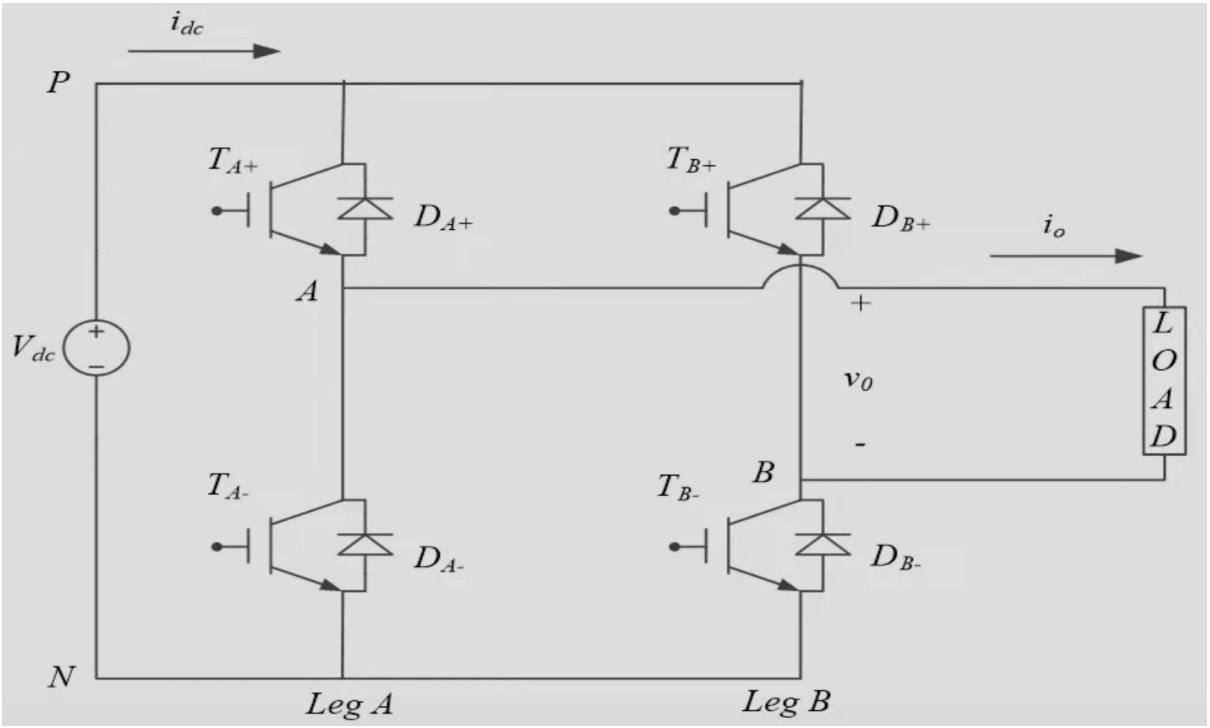


Figure 4.1: H - Bridge Topology

lower diodes, respectively. The DC bus is denoted by P and N, and the load is connected between these nodes. The voltage between A and B is denoted by Vo, and the load current is denoted by Io. The H bridge converter can be divided into four possible switching combinations: Ta + and Tb- are on together, Ta + and Tb + are diagonal switches, Ta + and Tb- are diagonal switches, Ta + and Tb + are diagonal switches, Ta + and Tb + are upper or lower switches, and Ta + and Tb + are both upper switches and Ta and Tb together.

To analyze each switching combination and their corresponding equivalent circuit, we can consider them shorted, as they are considered ideal. The equivalent circuit will be Vdc, with the output voltage named Vo being the one on. When the current direction is positive, the current flows through the transistor and back to the load. When the current direction is opposite, the current flows through the diodes and back to the load. When the current is negative, the current flows through the diode and back to the load.

The voltage across nonconducting devices must withstand Vdc because it is shorted to Vdc. Non-conducting devices must block Vdc and shorted Vdc, while conducting devices carry the current Io. This is important to remember, as we will use this information when drawing waveforms. In conclusion, the H bridge converter is a versatile and versatile converter that can be used in various applications. It has four IGBTs and four antiparallel diodes, with the potential for additional configurations depending on the application. By understanding the

different switching combinations and their equivalent circuits, we can better understand the design principles and applications of the H bridge converter.

On discussing the concept of pulse width modulation (PWM) in the context of H bridge converters. Focuses on four equivalent circuits, each representing a different type of current flow. The first circuit is called Vo, where the current is positive and flows downward to the negative terminal and positive to the positive terminal. The voltage is represented by Vo = -Vdc and Idc = -Io. When the current direction (Io) is positive, the devices that conduct are Da- and Db+. In contrast, when Io is negative, it flows in the opposite direction, carrying the devices Ta- and Tb+.The third switching combination is Vo, where both upper switches are turned on. The voltage is represented by Vo = 0 and Idc = 0. When the current direction is positive, the devices that conduct are Da+ and Tb+. When Io is negative, the conducting devices are Db+ and the diode Da+. The blocking voltages for non-conducting devices remain constant at Vdc. The fourth equivalent circuit is Ta- and Tb-, where the lower two switches are on. The path is followed by Vo = 0 and Idc = 0. When the current is positive, it flows downwards, while when it is negative, it flows upward. The gate pulse, also known as the gate pulse, is given to the gate of the IGBT or MOSFET.

As explained earlier there are two main types of PWM for H bridge converters: bipolar PWM, which uses the diagonal combinations Ta+ and Tb+, and unipolar PWM, which uses all four switching combinations. The modulation method used affects the voltage and current waveforms in different components and the design process. If the waveform changes, the device must withstand voltage, current, and frequencies, which affects the design accordingly. The key points are that when considering multiple switching combinations for a converter, it is essential to analyze the equivalent circuits for each possible switching combination to determine the different voltages and currents flowing through different devices and components. This helps in determining device ratings during the design process.

4.3 Schematic Designing

4.3.1 Power Stage Architecture

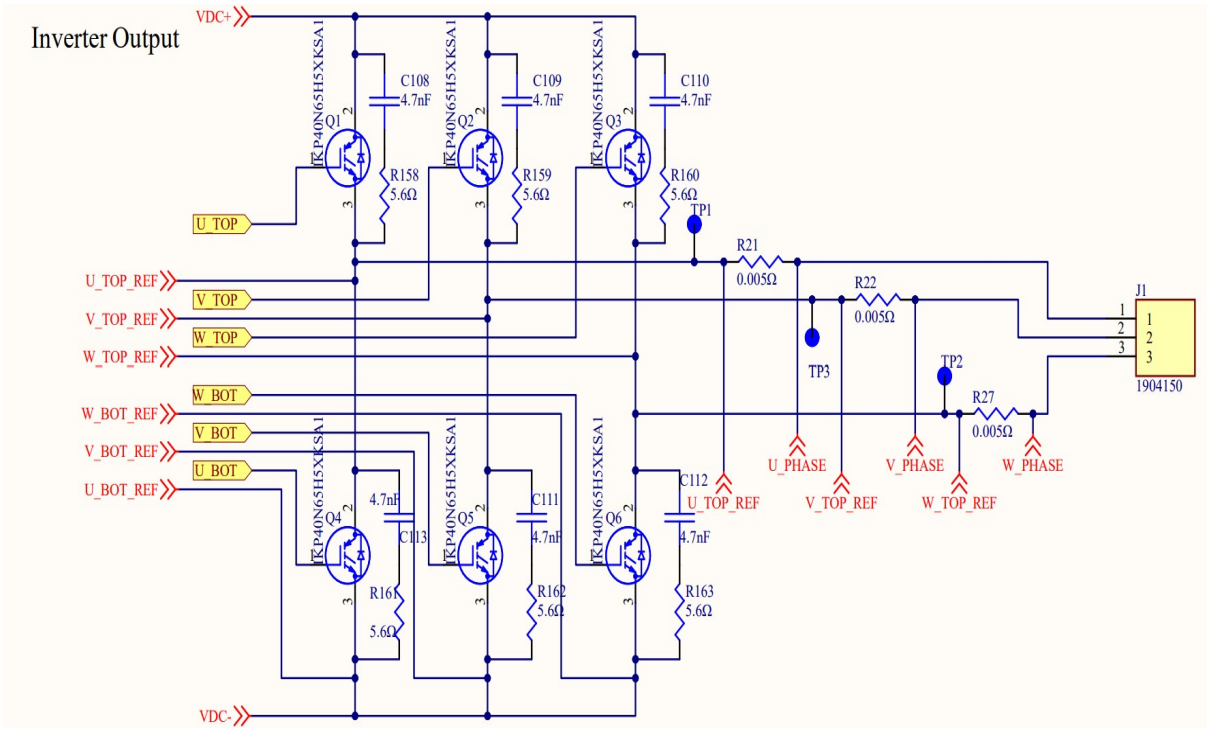


Figure 4.2: H - Bridge Design

The three-phase bridge inverter topology forms the core of modern power conversion systems. The six IGBTs (Q1-Q6) are arranged in a specific configuration to enable DC to AC conversion through controlled switching. The IKP40N65H5XKSA1 IGBTs used in this circuit are high-performance devices with several important characteristics.

- Voltage rating of 650V, suitable for industrial applications
- Low collector-emitter saturation voltage (VCE(sat)) to minimize conduction losses
- Fast switching capability to reduce switching losses
- Built-in anti-parallel freewheeling diodes to handle inductive load currents during commutation

The three half-bridge legs (U, V, W) operate with complementary switching - when the top switch is on, the bottom switch must be off, and vice versa. A small dead-time (typically a few microseconds) is implemented in the control signals to prevent shoot-through currents that

could damage the devices. Each leg generates one phase of the three-phase output, with the voltage at each output terminal switching between the positive and negative DC bus rails.

The physical layout of these components is critical, as they must be arranged symmetrically to ensure equal current distribution and thermal management. Power devices are typically mounted on heat sinks with thermal interface materials to dissipate the heat generated during operation.

1. DC Bus and Filtering: The DC bus structure is more sophisticated than might initially appear. The VDC+ and VDC- rails must maintain stable voltage during rapid current changes caused by switching events. The system typically includes the following.

- Large electrolytic bulk capacitors (not shown in the schematic) to store energy and maintain DC bus voltage
- Film capacitors placed close to the power modules for high-frequency decoupling
- The 4.7nF snubber capacitors (C108-C113) connected directly across each IGBT

These snubber capacitors serve specific purposes:

- Absorb energy stored in parasitic inductances during switching transitions
- Reduce voltage overshoot during turn-off, protecting the IGBTs from voltage spikes
- Slow down the rate of voltage change (dv/dt) to reduce electromagnetic interference
- Redistribute switching losses to improve thermal management

The size of these capacitors requires careful consideration of the switching frequency, DC bus voltage, and specific characteristics of the power devices. Too small and they will not effectively suppress transients; too large and they can increase switching losses.

2. Output connection: The three-phase output connector J1 (1904150) represents the interface to the load. This connection requires careful consideration:

- The connector must be rated for the maximum current and voltage of the application
- Wire gauge selection must account for current capacity, voltage drop, and thermal considerations

In motor drive applications, the output may connect to additional components such as

- Common mode chokes to reduce electromagnetic interference
- dv/dt filters to protect motor insulation from voltage stress
- Sine wave filters to produce smoother output waveforms

4.3.2 Gate Drive and Control Signals

The schematic shows a gate driver circuit for Phase U of a three-phase inverter system. This circuit is responsible for properly driving the high-side (top) and low-side (bottom) power transistors in the inverter's Phase U leg. Identical circuits would be implemented for phases V and W in a complete three-phase system. The heart of the circuit is the integrated circuit

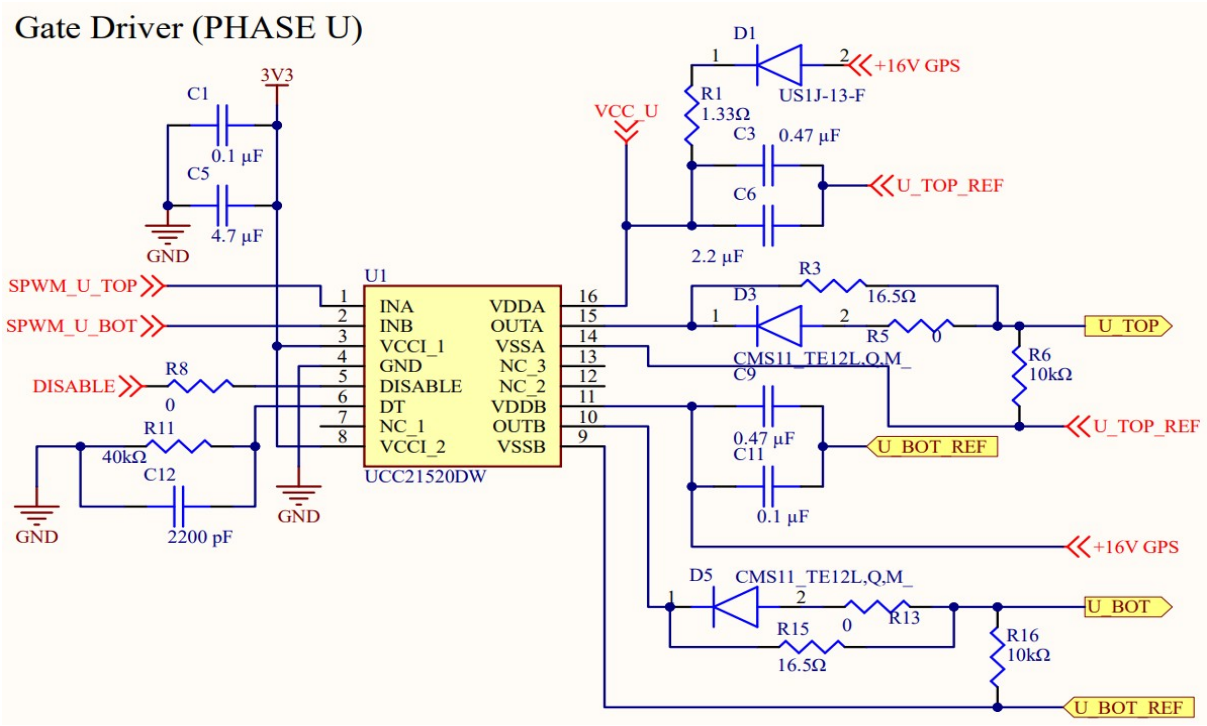


Figure 4.3: Gate Driver Design

UCC21520DW (U1), which is a dual-channel isolated gate driver specifically designed for high-voltage power switching applications. This IC provides the following.

- Galvanic isolation between the control signals and power stage
- Separate driving capability for both high-side and low-side switches
- Protection features to prevent shoot-through conditions
- High current drive capability for fast switching of power devices

The UCC21520DW has two input channels (INA and INB on pins 1 and 2) that receive the PWM control signals (SPWM_U_TOP and SPWM_U_BOT) from the controller. These signals determine the switching pattern of the power transistors. The outputs (OUTA and OUTB on pins 15 and 10) drive the gates of the power devices through additional circuitry.

1. Input Stage and Control:

   The input side of the gate driver includes several important components:

- PWM Signal Inputs: SPWM_U_TOP and SPWM_U_BOT signals enter the circuit and connect directly to the INA and INB pins of the UCC21520DW.
- Disable Function: A DISABLE signal connects to pin 5 through R8 (0Ω), allowing the controller to disable both outputs simultaneously for safety or during fault conditions.
- Input Power Supply: The circuit is powered by a 3V3 supply connected to capacitors C1 (0.1) and C5 (4.7), which provide filtering and decoupling.
- Dead-Time Control: The DT pin (pin 7) is connected to a timing network consisting of R11 (40$k\Omega$) and C12 (2200pF). This RC network sets the dead-time between the top and bottom switching signals to prevent shoot-through currents.

2. Output Stage and Gate Drive:

   The output stage for each switch contains several components:

i. High-Side (Top) Switch Drive Circuit:

- Isolation diode: D3 (CMS11_TE12L_QM) prevents reverse current flow
- Gate Resistor: R3 (16.5Ω) controls the turn-on/turn-off speed of the power transistor, balancing switching speed with noise and EMI considerations
- Zero-Ohm Resistor: R5 (0Ω) serves as a jumper that could be replaced with a resistor if needed for tuning the circuit
- Pull-Down Resistor: R6 (10$k\Omega$) ensures that the gate remains at a defined potential when not actively driven
- Feedback Network: The U_TOP_REF signal provides feedback to the control system.

ii. Low-Side (Bottom) Switch Drive Circuit:

- Isolation diode: D5 (CMS11_TE12L_QM) prevents reverse current flow
- Gate Resistor: R15 (16.5Ω) controls switching characteristics
- Zero-Ohm Resistor: R13 (0Ω) serves as a jumper
- Pull-Down Resistor: R16 ($10k\Omega$) ensures a defined gate potential when not driven
- Feedback Network: The U_BOT_REF signal provides feedback to the control system.

3. Power Supply and Filtering

The circuit includes sophisticated power supply and filtering components:

i. High-Side Power Supply:

- VCC_U supplies power to the high-side driver circuitry
- D1 (US1J-13-F) rectifies the +16V GPS supply
- R1 (1.33Ω) limits inrush current
- C3 (0.47μF) and C6 (2.2μF) filter the supply voltage

ii. Output Filtering:

- C9 (0.47μF) and C11 (0.1μF) provide filtering for the low-side driver output
- These capacitors help reduce noise and ensure clean switching signals

4. Generalized Implementation for the Three-Phase System In a complete three-phase inverter system, this gate driver circuit would be replicated three times, one for each phase (U, V and W). The only differences would be the signal names:

- Phase U: SPWM_U_TOP, SPWM_U_BOT, U_TOP, U_BOT, U_TOP_REF, U_BOT_REF, VCC_U
- Phase V: SPWM_V_TOP, SPWM_V_BOT, V_TOP, V_BOT, V_TOP_REF, V_BOT_REF, VCC_V
- Phase W: SPWM_W_TOP, SPWM_W_BOT, W_TOP, W_BOT, W_TOP_REF, W_BOT_REF, VCC_W

5. Technical Considerations and Design Rationale

- Isolation strategy: The UCC21520DW provides reinforced galvanic isolation between the control circuitry and the power stage, which is critical for safety and noise immunity. This isolation protects the low-voltage control electronics from the high voltages present in the power stage.
- Dead-Time Implementation: The dead-time circuit (R11 and C12) ensures that both the high-side and the low-side switches are never on simultaneously, preventing destructive shoot-through currents. The $40k\Omega$ resistor and 2200pF capacitor create a time constant that determines the minimum delay between the switching transitions.
- Gate Drive Optimization: The 16.5Ω gate resistors (R3 and R15) are carefully selected to balance:
  - Switching speed (faster switching reduces losses but increases EMI)
  - Gate current peaks (limited to protect the driver IC)
  - Ringing and oscillation (damped to prevent false triggering)
- Thermal Considerations: The zero ohm resistors (R5 and R13) allow for future adjustment if thermal testing indicates the need to slow down the switch to reduce losses.
- Feedback Implementation: The reference signals (U_TOP_REF and U_BOT_REF) provide feedback to the control system for monitoring and protection purposes. These signals can be used to detect fault conditions such as short circuits or open circuits.
- Power Supply Filtering: Multiple capacitors with different values (0.1, 0.47, 2.2, 4.7) are used to filter different frequency ranges of noise, ensuring stable operation throughout the frequency spectrum.

This gate driver design represents a robust and industry-standard approach to driving power semiconductors in three-phase inverter applications, with careful attention to isolation, protection, switching performance, and noise immunity.

4.3.3 Current Sensing

The schematic shows a sophisticated current sensing circuit for Phase U of a three-phase inverter system. This circuit is designed to accurately measure the current flowing through the

power stage and provide protection against over-current conditions. An identical circuit would be implemented for phases V and W in a complete three-phase system.

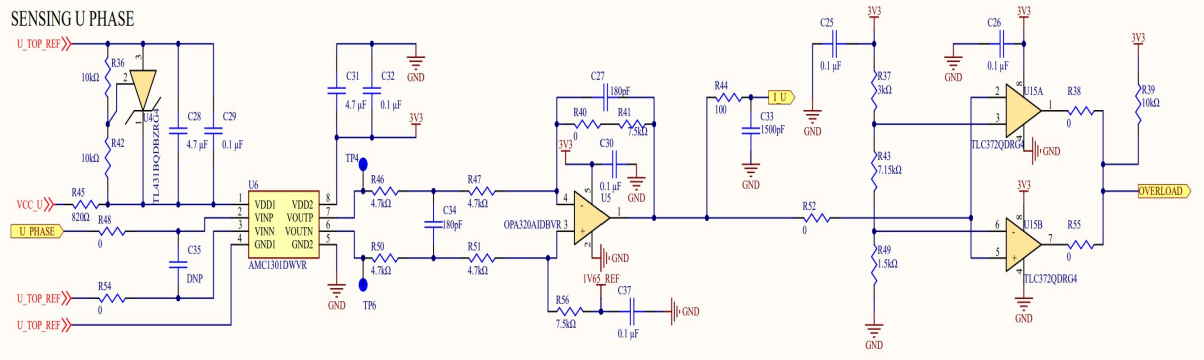


Figure 4.4: Current Sensing Circuit

1. Input Stage and Signal Conditioning

The circuit begins with the U_TOP_REF and U_PHASE input signals that represent the voltage across the current sensing shunt resistor in the power stage. These signals enter through two paths:

i. Differential Amplifier Input:

- U_TOP_REF connects through a $10k\Omega$ resistor (R41) to the non-inverting input
- U_PHASE connects through a 0Ω resistor (R48) to the AMC1301DWVR isolation amplifier

ii. Buffer Stage:

- U_TOP_REF also connects through a $10k\Omega$ resistor (R42) to a TL431AIDBZR2G precision shunt regulator (U2)
- This creates a buffered reference signal

The TL431AIDBZR2G (U2) acts as a voltage reference and buffer, with supporting components:

- $10k\Omega$ resistors (R41, R42) for biasing
- Decoupling capacitors C28 (4.7) and C29 (0.1) for stable operation
- VCC_U supplies power to this stage

2. Isolation Amplifier Stage

At the core of the sensing circuit is the AMC1301DWVR (U6), a precision isolated amplifier specifically designed for current shunt measurement in high-voltage systems. This component:

- Provides galvanic isolation between the power circuit and control electronics
- Has high common-mode rejection for accurate measurements in noisy environments
- Features a differential input for connecting across the shunt resistor

The AMC1301 connections include:

- VIN+ and VIN- (pins 2 and 3) for differential input
- VOUT+ and VOUT- (pins 7 and 6) for differential output
- VDD1 and GND1 (pins 1 and 4) for input-side power
- VDD2 and GND2 (pins 8 and 5) for output-side power

Power and filtering components include:

- C31 ($4.7F$) and C32 ($0.1F$) for input-side power filtering
- C35 (DNP - Do Not Populate) placeholder for additional filtering if needed
- 3V3 supply powers the output side of the isolation barrier

3. Differential to Single-Ended Conversion

The differential output of the isolation amplifier is converted to a single-ended signal using an OPA320AIDBVR3 (U7) precision operational amplifier configured as a differential amplifier:

- R46 and R47 (both $4.7k\Omega$) connect to the differential outputs of the AMC1301
- R50 and R51 (both $4.7k\Omega$) provide feedback and set the gain
- C34 is connected across R50 to form a low-pass filter, reducing high-frequency noise
- Test points TP4 and TP6 allow for signal measurement during testing and calibration

The OPA320AIDBVR3 features the following:

- Low noise for accurate signal reproduction
- High precision for reliable current measurement
- Rail-to-rail output for maximum dynamic range

4. Reference and Filtering

The circuit includes a reference voltage generation section:

- R56 ($7.5k\Omega$) and C37 (0.1μF) create a filtered reference voltage (VGCC_REF)
- C30 (0.1μF) provides additional filtering for the op-amp
- C27 (180pF) and R44 (10Ω) form an RC filter to reduce high-frequency noise

5. Comparison stage for overcurrent protection

The final section features two TLC372QDRG4 comparators (U15A and U15B) that implement overcurrent protection.

i. First Comparator (U15A):

- The processed current signal connects to the inverting input (pin 2)
- A reference threshold set by R37 ($2k\Omega$) and R43 ($7.15k\Omega$) connects to the non-inverting input (pin 3)
- Output (pin 1) connects through R38 (0Ω) to the second comparator

ii. Second comparator (U15B):

- Input from the first comparator connects to the non-inverting input (pin 5)
- R49 ($1.5k\Omega$) provides positive feedback for hysteresis
- Output (pin 7) provides the OVERLOAD signal to the control system

Supporting components include:

- C25, C26 (both 0.1μF) for the decoupling of the power supply
- R39 ($10k\Omega$) as a pull-up resistor
- R52 and R55 (both 0Ω) allow for circuit tuning if needed

6. Generalized Implementation for the Three-Phase System In a complete three-phase inverter system, this sensing circuit would be replicated three times with identical component values but different signal names:

- Phase U: U_TOP_REF, U_PHASE, VCC_U
- Phase V: V_TOP_REF, V_PHASE, VCC_V
- Phase W: W_TOP_REF, W_PHASE, VCC_W

Each phase would have its own OVERLOAD signal that could be combined in the control system to trigger appropriate protective actions.

7. Technical Design Considerations

- Isolation strategy: The AMC1301 provides reinforced galvanic isolation (up to 7kV) between the high-voltage power stage and low-voltage control electronics, protecting the control system and ensuring measurement accuracy.
- Precision Measurement: The combination of precision components ensures accurate current measurement:
  - The AMC1301 has a typical gain error of less than 0.5%
  - The OPA320 has a low offset voltage (typically <150μV)
  - Matched resistor values maintain balanced differential signal paths
- Noise Immunity: Multiple filtering stages reduce measurement noise:
  - input and output decoupling capacitors
  - strategic placement of bypass capacitors RC filters at critical nodes
  - differential signaling throughout most of the circuit
- Overcurrent protection: The dual-comparator design with hysteresis provides reliable overcurrent detection with:
  - Fast response time (typically <1μs)
  - Adjustable threshold via resistor values
  - Hysteresis to prevent oscillation at the threshold boundary

  - Direct OVERLOAD signal output for immediate protective action

- Layout Considerations: Though not visible in the schematic, the physical implementation would require:

  - Careful separation of high-voltage and low-voltage sections
  - Short traces for high-frequency signals
  - Proper grounding to prevent ground loops
  - Shielding to minimize electromagnetic interference

This current sensing circuit represents a professional-grade design that balances accuracy, noise immunity, and protection capabilities, essential for the reliable operation of high-power three-phase inverter systems in industrial applications, motor drives, or renewable energy systems.

4.3.4 Sensing circuit for DC Link Voltage

The schematic shows a sophisticated DC link voltage sensing circuit designed for a three-phase inverter system. This circuit provides accurate measurement of the high voltage DC bus while maintaining galvanic isolation between the power stage and control electronics.

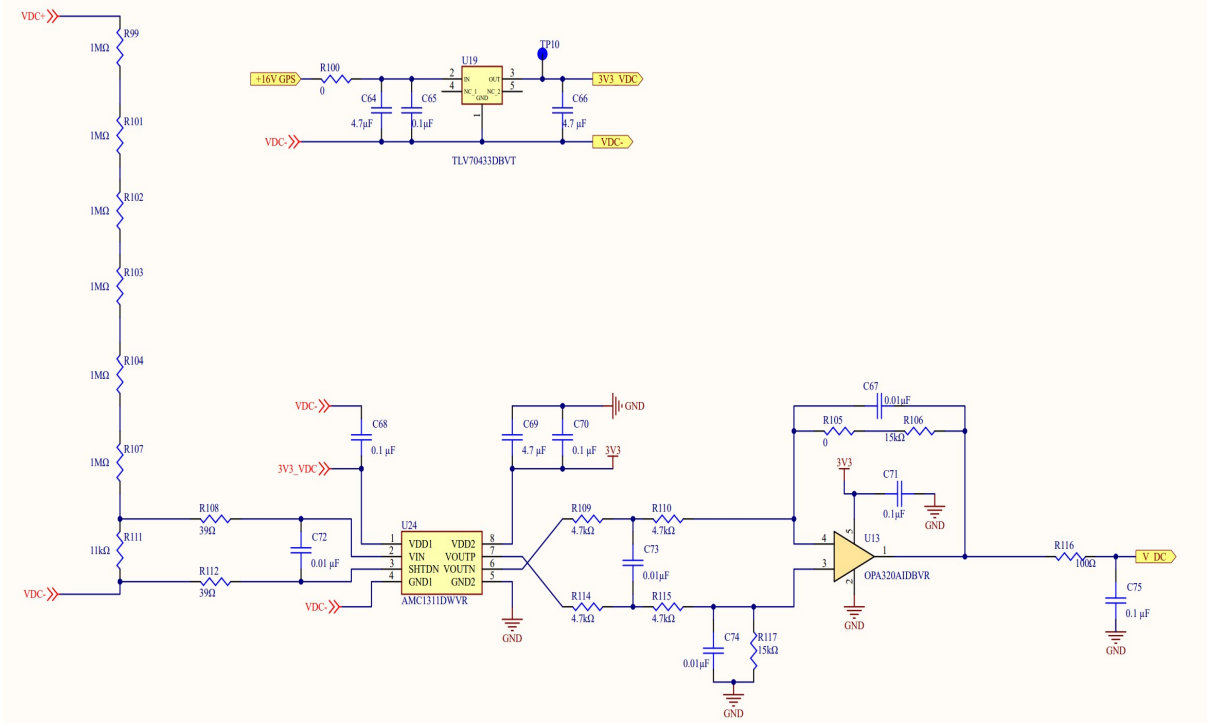


Figure 4.5: DC Link Voltage Sensing Circuit

1. Voltage Divider Network

The left side of the schematic features a high-impedance voltage divider network consisting of:

- Six $1M\Omega$ resistors (R99, R101, R102, R103, R104, R107) connected in series
- An $11k\Omega$ resistor (R111) at the bottom of the divider chain

This resistor network scales the high DC link voltage (VDC +) to a manageable level for the isolation amplifier. The high total resistance ($6M\Omega + 11k\Omega$) ensures minimal loading on the DC bus while providing appropriate voltage division. The design uses multiple high-value resistors in series rather than a single resistor to distribute the voltage stress and improve reliability in high-voltage applications.

2. Power Supply Section

At the top of the schematic, there is a power supply section built around the TLV70433DBVT low-dropout regulator (U19):

- Input: +16V GPS (Gate Power Supply)
- Output: 3V3_VDC (3.3V regulated supply)
- R100 (0Ω) serves as a jumper or current-limiting option
- Input filtering: C64 (4.7μF) and C65 (0.1μF) capacitors
- Output filtering: C66 (4.7μF) capacitor
- Test point TP10 allows voltage measurement during testing

This regulated 3.3V supply powers the isolation and signal conditioning components.

3. Isolation Amplifier Stage

The core of the sensing circuit is the AMC1311DWVR (U24), a precision isolated delta sigma modulator specifically designed for voltage sensing in high-voltage systems.

- VDD1 (pin 1) and GND1 (pin 4) connect to the high-voltage side
- VDD2 (pin 8) and GND2 (pin 5) connect to the isolated low-voltage side
- VIN (pin 2) receives the divided down DC-link voltage

- SHDN (pin 3) is the shutdown input (connected to VDC-)
- VOUTP (pin 6) and VOUTN (pin 7) provide differential output signals

4. Power filtering components include:

- C68 (0.1μF) on the high-voltage side
- C69 (4.7μF) and C70 (0.1μF) on the low-voltage side

5. Differential to Single-Ended Conversion

The differential output from the isolation amplifier is converted to a single-ended signal using an OPA320AIDBVR (U13) precision operational amplifier configured as a differential amplifier:

- R109 and R110 (both 4.7$k\Omega$) connect to the differential outputs of the AMC1311
- R114 and R115 (both 4.7$k\Omega$) provide feedback and set the gain
- C73 (0.01μF) provides filtering
- R117 (15$k\Omega$) and C74 (0.01μF) form an additional filter network
- R105 (0Ω) and R106 (15$k\Omega$) set up the reference level
- C67 (0.01μF) provides additional filtering
- R116 (10$k\Omega$) and C75 (0.1μF) form an output filter

6. Signal Conditioning and Buffering

The final output stage includes:

- C71 (0.1μF) for power supply decoupling of the op-amp
- Output labeled V_DC represents the conditioned DC-link voltage signal ready for the ADC input

7. Technical Design Considerations

- Isolation strategy: The AMC1311 provides reinforced galvanic isolation between the high-voltage DC bus and low-voltage control electronics, protecting the control system and ensuring measurement accuracy. This isolation is critical for safety in high-power applications

- Precision Scaling: The resistor divider network is carefully designed to scale the DC-link voltage (which can be up to 1026V according to similar designs) down to the input range of the isolation amplifier (0-2V for optimal performance)
- Noise Immunity: Multiple filtering stages reduce measurement noise:
  - Input and output decoupling capacitors
  - Strategic placement of bypass capacitors
  - RC filters at critical nodes
  - Differential signaling throughout most of the circuit
- High Input Impedance: The $6M\Omega$ total resistance of the divider network ensures minimal loading on the DC bus, which is important for accurate voltage measurement and efficiency
- Protection Features: Although not explicitly shown, high-value resistors in the divider network provide inherent current limiting in the event of faults. In some implementations, Zener diodes would be added in parallel with some resistors for overvoltage protection.

This DC link voltage sensing circuit represents a professional-grade design that balances accuracy, safety through isolation, and noise immunity. It is essential for proper control and protection of the inverter system, enabling functions such as over-voltage protection, under-voltage detection, and precise control of power conversion processes.

4.3.5 DC LINK TEMPERATURE SENSING CIRCUIT

The schematic shows a sophisticated DC link temperature sensing circuit designed to accurately measure the temperature of the DC bus in a power electronics system while maintaining galvanic isolation between the power stage and control electronics.

1. Input Stage and NTC Interface

The circuit begins with an NTC (Negative Temperature Coefficient) thermistor input on the left side. This thermistor is the actual temperature sensing element physically mounted on the DC link capacitor or bus bar. Key components in this stage include:

- Two 39Ω resistors (R120 and R123) connected in series with the NTC thermistor input
- A 0.01μF capacitor (C81) for noise filtering at the input

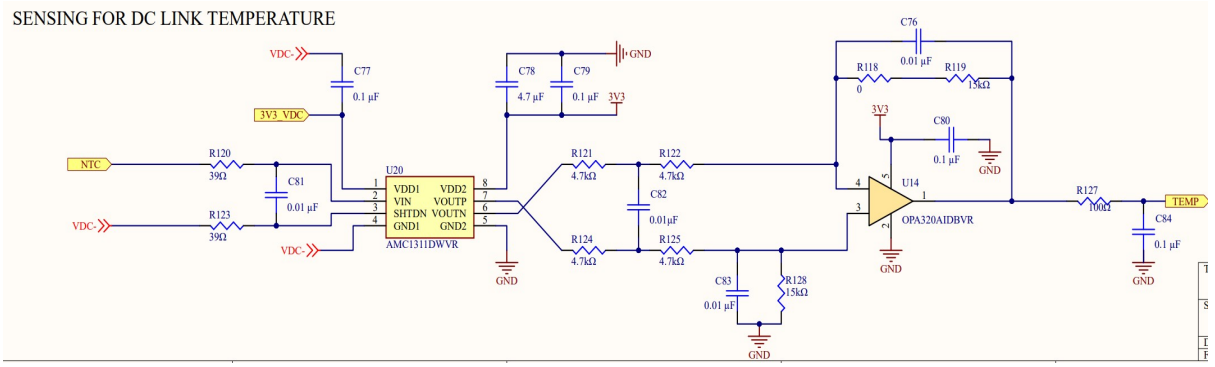


Figure 4.6: DC Link Voltage Sensing Circuit

- The NTC thermistor's resistance varies inversely with temperature, providing the primary sensing function

This configuration allows the circuit to read the resistance change of the NTC thermistor, which is directly correlated to the temperature changes in the DC link.

2. Isolation Amplifier Stage

At the core of the sensing circuit is the AMC1311DWVR (U20), a precision isolated delta-sigma modulator specifically designed for voltage sensing with galvanic isolation:

- VDD1 (pin 1) and GND1 (pin 4) connect to the high-voltage side
- VDD2 (pin 8) and GND2 (pin 5) connect to the isolated low-voltage side
- VIN (pin 2) receives the voltage signal from the NTC thermistor network
- SHDN (pin 3) is the shutdown input (connected to VDC-)
- VOUTP (pin 6) and VOUTN (pin 7) provide differential output signals

The isolation amplifier is powered by:

- 3V3_VDC supply on the high-voltage side with C77 (0.1μF) for filtering
- 3V3 supply on the low-voltage side with C78 (4.7μF) and C79 (0.1μF) for filtering

This isolation barrier is crucial for safety, separating the high-voltage power circuit from the low-voltage control electronics.

3. Differential to Single-Ended Conversion

The differential output from the isolation amplifier is converted to a single-ended signal using a precision signal conditioning network:

- Four $4.7k\Omega$ resistors (R121, R122, R124, R125) form a differential amplifier configuration.
- C82 (0.01μF) provides filtering for the differential signal
- R128 ($15k\Omega$) and C83 (0.01μF) form an additional filter network

4. Signal Conditioning and Amplification

The final stage uses an OPA320AIDBVR (U14) precision operational amplifier configured as a non-inverting amplifier:

- The op-amp is powered by the 3V3 supply with C80 (0.1μF) for power supply decoupling
- R118 (0Ω) serves as a jumper
- R119 ($1M\Omega$) provides high input impedance
- C76 (0.01μF) forms an input filter with R119
- The output is filtered by R127 (100Ω) and C84 (0.1μF)
- The final output is labeled T_TEMP, representing the conditioned temperature signal

5. Technical Design Considerations

- Isolation strategy: The AMC1311 provides reinforced galvanic isolation between the high-voltage DC link and low-voltage control electronics, protecting the control system and ensuring measurement accuracy. This isolation is critical for safety in high-power applications
- Temperature Measurement Principle: The circuit measures the voltage across the NTC thermistor, which changes with temperature. As the temperature increases, the thermistor's resistance decreases, altering the voltage division ratio in the input network.
- Noise Immunity: Multiple filtering stages reduce measurement noise:
  - Input filtering with C81
  - Power supply decoupling capacitors throughout the circuit
  - Strategic RC filters at critical signal path points

  - Differential signaling through the isolation barrier

- Signal Conditioning: The op-amp stage provides the following:

  - Impedance matching between the isolation amplifier and subsequent ADC stages
  - Additional filtering to improve signal quality
  - Appropriate scaling of the temperature signal for the control system's input range

- Robustness: The 39Ω series resistors (R120 and R123) provide current limiting protection for the input stage, while the multiple filter capacitors enhance immunity to electrical noise in the harsh switching environment of power electronics.

This DC link temperature-sensing circuit represents a professional-grade design that balances accuracy, safety through isolation, and noise immunity. Temperature monitoring is essential for the protection of power components, as excessive temperatures can lead to premature failure or catastrophic breakdown of semiconductor devices and DC link capacitors. The circuit enables the control system to implement thermal protection algorithms, adjust switching patterns to reduce thermal stress, or shut down the system if temperatures exceed safe operating limits.

4.3.6 Phase Monitoring and Fault Detection

The schematic shows a sophisticated ground fault detection circuit designed to monitor the three-phase currents (I_U, I_V, I_W) in a power inverter system and detect imbalances that could indicate ground faults or other abnormal conditions. 1. Input Stage and Signal Summation

The circuit begins with three input signals representing the phase currents:

- I_U: Phase U current signal
- I_V: Phase V current signal
- I_W: Phase W current signal

Each input signal passes through a $10k\Omega$ resistor (R144, R145, R146) before being summed at a common node. This resistor network creates a signal averaging function that combines the three phase currents. In a balanced three-phase system with no ground fault, the sum of these currents should theoretically be zero (or very close to zero) due to Kirchhoff's Current Law.

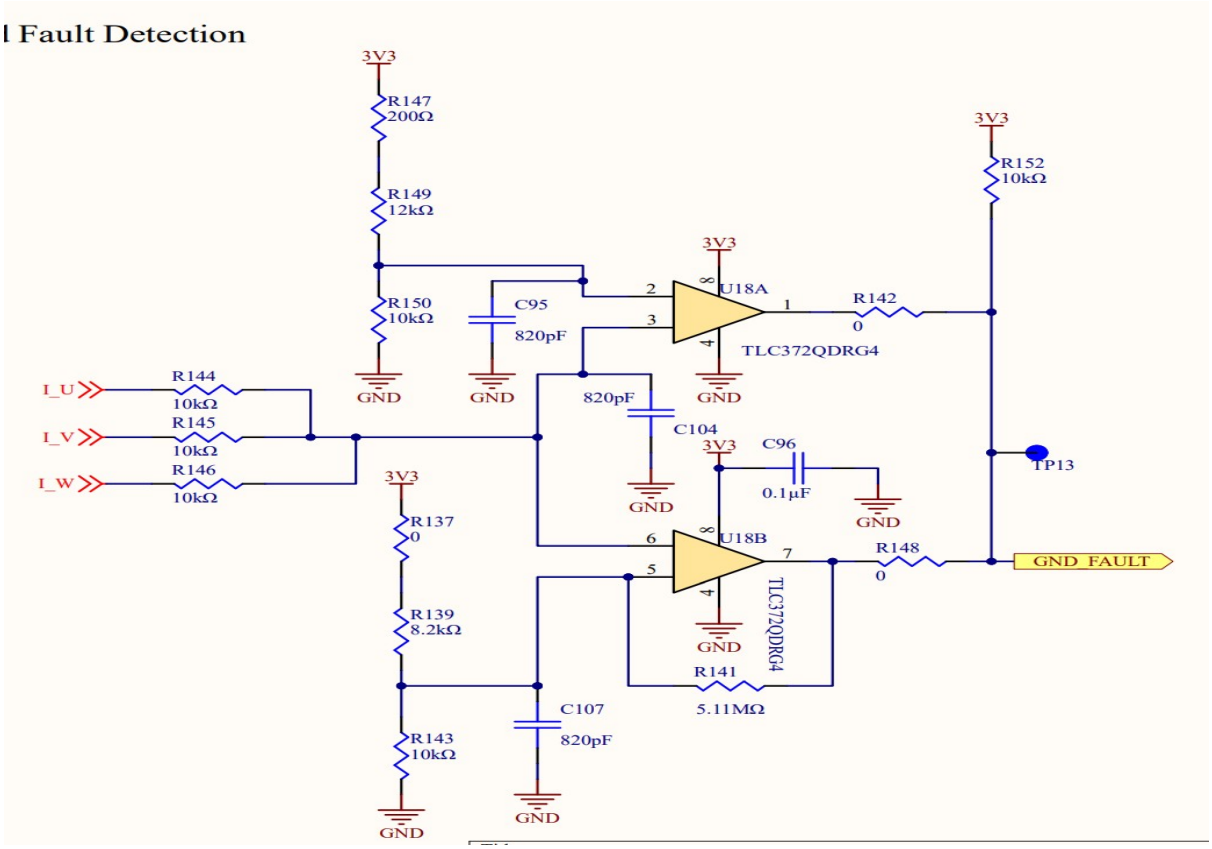


Figure 4.7: Phase Monitoring and Fault Detection Circuit

2. Upper Comparator Circuit (U18A)

The upper portion of the circuit features a TLC372QDRG4 comparator (U18A) with these key components:

i. Reference Voltage Divider:

- A voltage divider consisting of R147 (200Ω), R149 (12kΩ), and R150 (10kΩ) connected between 3V3 and ground
- This creates a precise reference voltage at the non-inverting input (pin 3)

ii. Input Filtering:

- C95 (820pF) capacitor provides noise filtering at the non-inverting input
- C104 (820pF) capacitor filters the inverting input (pin 2)

iii. Output Stage:

- R142 (0Ω) connects the output (pin 1) to the fault signal line
- R152 (10kΩ) serves as a pull-up resistor to 3V3

3. Lower Comparator Circuit (U18B)

The lower portion of the circuit features the second comparator in the TLC372 package (U18B):

i. Reference Voltage Divider:

- A voltage divider consisting of R137 (0Ω), R139 ($8.2k\Omega$), and R143 ($10k\Omega$) connected between 3V3 and ground
- This creates a second reference voltage at the non-inverting input (pin 5)

ii. Input Filtering:

- C107 (820pF) capacitor provides noise filtering at the non-inverting input
- C96 (0.1μF) capacitor connected to 3V3 provides additional filtering

iii. Feedback Network:

- R141 ($5.11M\Omega$) provides positive feedback for hysteresis, creating a Schmitt trigger configuration
- This prevents oscillation when the input signal is near the threshold

iv. Output stage:

- R148 (0Ω) connects the output (pin 7) to the GND_FAULT signal line
- Test point TP13 allows for signal measurement during testing and debugging

4. Technical Operation and Design Considerations

- Fault Detection Principle: The circuit operates on the principle that in a balanced three-phase system, the sum of the three-phase currents should equal zero. Any significant deviation from zero indicates a potential ground fault or phase imbalance.
- Dual-threshold detection: The dual comparator arrangement creates a window comparator that can detect when the summed signal goes either above or below preset thresholds. This allows detection of both positive and negative imbalances in the three-phase system

- Hysteresis Implementation: The 5.11$M\Omega$ feedback resistor (R141) in the lower comparator creates hysteresis, which prevents the rapid osmotic movement of the fault signal when the input hovers near the threshold. The precise value (5.11$M\Omega$) suggests a careful calculation to achieve specific hysteresis characteristics.

- Noise Immunity: Multiple filtering capacitors (820pF and 0.1μ F) in strategic locations reduce the impact of switching noise. The resistor values are chosen to provide appropriate time constants for filtering while maintaining sensitivity.

- Reference Voltage Precision: The voltage divider networks are designed to create precise threshold voltages The 200Ω/12$k\Omega$/10$k\Omega$ and 0Ω/8.2$k\Omega$/10$k\Omega$ combinations create different threshold levels for the upper and lower limits.

This ground fault detection circuit represents a professional-grade design that provides critical protection in three-phase power systems. By continuously monitoring the balance of phase currents, it can quickly detect ground faults or other abnormal conditions that could damage equipment or create safety hazards. The GND_FAULT signal would typically connect to the system controller to trigger protective actions such as shutting down the inverter or activating alarms.

4.3.7 DC Input Power Supply

The schematic shows a DC input circuit for a three-phase inverter system. This circuit represents the DC power entry point and includes temperature-sensing and connection components that form the foundation of the inverter's power stage.

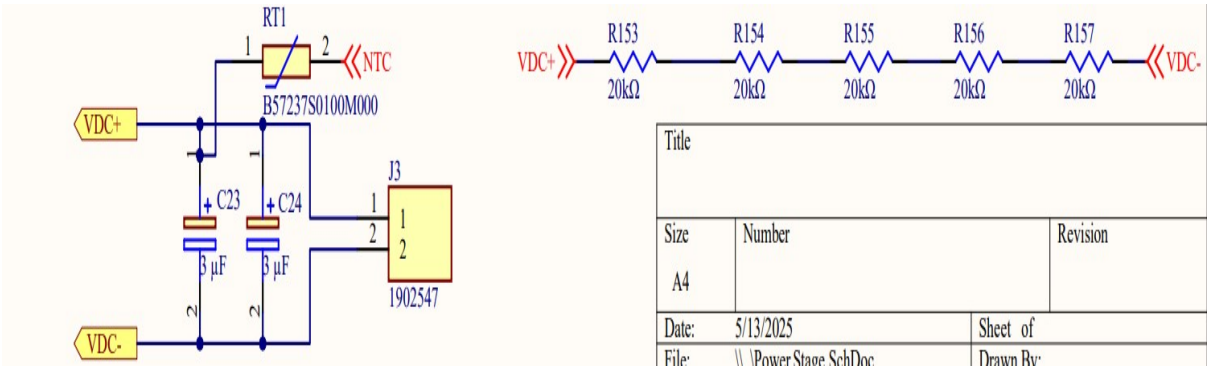


Figure 4.8: DC Power Supply Circuit

1. DC Input Power Stage

The left side of the schematic shows the main DC power input section:

i. DC Bus Connections:

- VDC+ and VDC- terminals serve as the primary DC power input connections
- These terminals would connect to a DC power source such as batteries, a rectified AC supply, or solar panels
- The DC bus voltage would typically be in the range of several hundred volts for industrial inverters

ii. Filtering Capacitors:

- Two 3μF capacitors (C23 and C24) are connected in parallel between VDC+ and VDC-
- These capacitors serve multiple critical functions:
  - Filtering high-frequency noise and ripple from the DC input
  - Providing local energy storage to handle current transients during switching events
  - Stabilizing the DC bus voltage during rapid load changes
- The value of 3μ F suggests that these are likely film capacitors rather than electrolytic capacitors, chosen for their superior high-frequency performance and reliability.

The value of 3μ F suggests that these are probably film capacitors rather than electrolytic capacitors, chosen for their superior high-frequency performance and reliability.

2. Temperature-Sensing Circuit

The center of the schematic features a temperature sensing element:

i. NTC Thermistor:

- RT1 (B57237S0100M000) is an NTC (Negative Temperature Coefficient) thermistor
- This component's resistance decreases as temperature increases
- It's strategically placed to monitor the temperature of the DC link components
- The specific B57237S0100M000 model is likely a 10$k\Omega$ (at 25°C) precision thermistor with a specific B-constant for accurate temperature measurement

ii. Thermistor connections:

- The thermistor is connected between pins 1 and 2
- Pin 2 is labeled "NTC" and would connect to the temperature sensing circuit elsewhere in the system
- This allows the control system to monitor the DC link temperature for protection and thermal management

iii. Output Connector

The schematic includes a connector for external connections:

1. Connector J3:

- J3 (1902547) is a 2-pin connector
- Pin 1 connects to the thermistor
- Pin 2 connects to VDC-
- This connector likely provides the temperature sensing signal to the control board

3. DC Bus Voltage Divider

The right side of the schematic shows a resistor network:

i. Voltage Divider Chain:

- Five $20k\Omega$ resistors (R153, R154, R155, R156, R157) are connected in series between VDC+ and VDC-
- This forms a voltage divider that scales down the high DC bus voltage
- The total resistance ($100k\Omega$) limits current draw while providing sufficient signal for measurement
- Using multiple resistors in series distributes the voltage stress across multiple components, improving reliability and safety

4. Technical Design Considerations

- Voltage Rating:
  - All components must be rated for the maximum DC bus voltage plus safety margin

  - The multiple resistors in series ensure no single component experiences the full DC bus voltage

- Temperature Monitoring Strategy:
  - The NTC thermistor placement is critical for detecting potential overheating conditions
  - It's likely positioned near the DC link capacitors or power semiconductors, which are typically the most thermally stressed components
- Safety Considerations:
  - The resistor divider provides a means to safely measure the high DC bus voltage
  - The capacitors include proper voltage ratings and safety margins to prevent catastrophic failures
- Filtering performance:
  - The 3μF capacitors are sized to handle the expected ripple current and provide adequate filtering
  - The parallel configuration reduces the effective ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance)

This DC input circuit represents a well-designed power entry stage for a three-phase inverter system, with attention to filtering, temperature monitoring, and voltage measurement. These features are essential to ensure reliable and safe operation of the inverter under various operating conditions.

4.3.8 Voltage Regulation

The schematic shows a comprehensive voltage regulation system for an inverter circuit, featuring multiple voltage regulation stages and reference voltage generation. This circuit is responsible for creating stable power supply voltages required by the control and sensing circuits in the inverter system. 1. Input Power and Primary Regulation Stage

The left side of the schematic shows the primary power input and first regulation stage:

i. Power Input Connector:

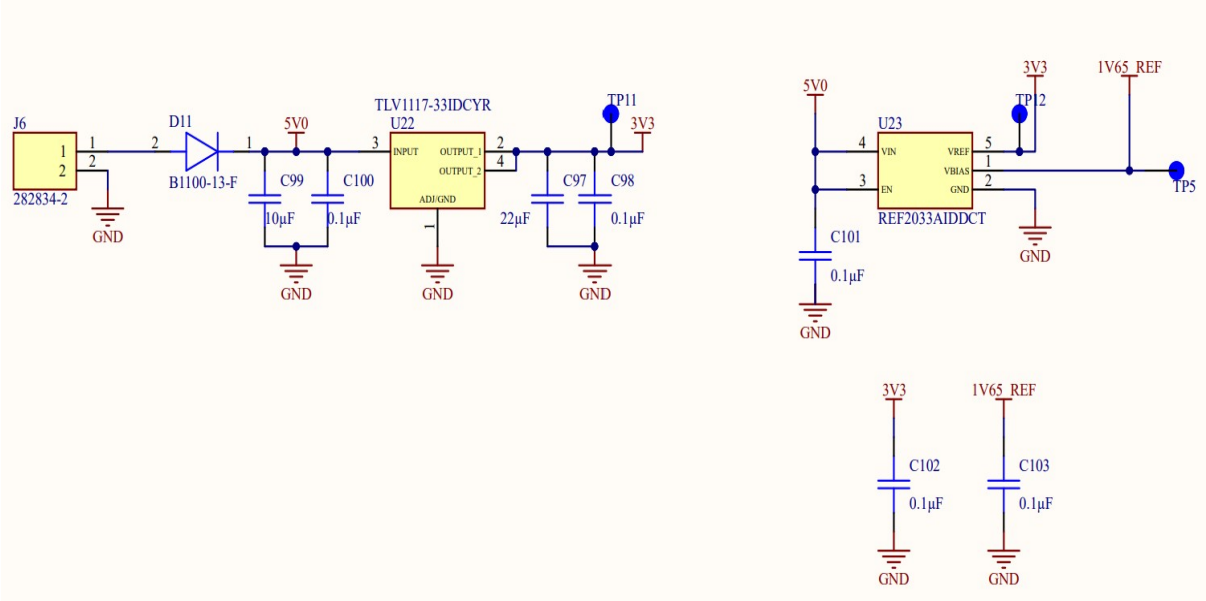


Figure 4.9: Voltage Regulation Circuit

- J6 is a 2-pin connector (282834-2) that serves as the primary power input
- Pins 1 and 2 are connected together, suggesting a single power input with redundant pins for current handling

ii. Rectification Stage:

- D11 (B1100-13-F) is a diode that provides reverse polarity protection
- This diode prevents damage if the input power is connected with reversed polarity
- The B1100-13-F is likely selected for its appropriate voltage rating and low forward voltage drop to minimize power loss

iii. Input Filtering:

- C99 (10μF) provides bulk filtering of the input supply
- C100 (0.1μF) filters high-frequency noise
- This combination of capacitors ensures a clean input to the voltage regulator

iv. First Regulator Stage:

- U22 (TLV1117-33IDCYR) is a low-dropout (LDO) linear voltage regulator
- This regulator converts the input voltage (likely 5V based on the 5V0 label) to 3.3V

- The TLV1117 series features:
  - 800mA output current capability
  - Low dropout voltage (typically 1.2V at full load)
  - Built-in current limiting and thermal shutdown protection
- The regulator has dual outputs (OUTPUT_1 and OUTPUT_2) for flexibility in power distribution.

v. Output Filtering:

- C97 (22μF) provides bulk filtering of the 3.3V output
- C98 (0.1μF) filters high-frequency noise
- This combination ensures a stable 3.3V supply (labeled 3V3)
- Test point TP11 allows for voltage measurement during testing and debugging

2. Precision Voltage Reference Stage

The right side of the schematic shows a precision voltage reference circuit:

i. Voltage Reference IC:

- U23 (REF2033AIDDCT) is a precision voltage reference IC
- This component provides a highly accurate and stable reference voltage
- The REF2033A features:
  - 3.0V ±0.05% initial accuracy output
  - Very low temperature drift (typically 3ppm/°C)
  - Low noise output (typically 3.0μVpp)
  - Low quiescent current (40μA typical)

ii. Input and control:

- VIN (pin 4) is connected to the 5V0 supply
- EN (pin 3) is the enable pin, connected to ground to keep the reference always enabled

- VBIAS (pin 2) is internally connected in the IC

iii. Output Configuration:

- VREF (pin 5) provides the precision reference voltage (labeled 1V65_REF, suggesting a 1.65V reference)
- Test point TP12 allows for measurement of the 3V3 supply
- Test point TP5 allows for measurement of the 1V65_REF output

iv. Additional Filtering:

- C101 (0.1μF) provides filtering for the reference IC
- C102 (0.1μF) provides additional filtering for the 3V3 supply
- C103 (0.1μF) provides filtering for the 1V65_REF output
- These capacitors ensure stable, noise-free reference voltages

3. Technical Design Considerations

i. Power Supply Hierarchy:

- The circuit creates a hierarchical power structure:
- Input power (likely 5V) $\rightarrow$ 3.3V regulated supply $\rightarrow$ 1.65V precision reference
- This cascade ensures each subsequent stage has a cleaner power source

ii. Reference Voltage Selection:

- The 1.65V reference (1V65_REF) is likely chosen to serve as a mid-supply reference for analog circuits
- This value is exactly half of 3.3V, making it ideal for biasing differential amplifiers and ADC reference inputs

iii. Noise Reduction Strategy:

- Multiple decoupling capacitors at different values (0.1μF, 10μF, 22μF) target different frequency ranges of noise

- The smaller capacitors (0.1μF) handle high-frequency noise while larger values address lower frequency variations
- The precision reference IC inherently provides low-noise performance

iv. Thermal Considerations:

- The TLV1117 regulator may require thermal management if the voltage drop from input to output is significant.
- The REF2033A has low self-heating due to its low quiescent current

v. Stability Assurance:

- The capacitor values are selected to ensure stability of the regulators
- The TLV1117 typically requires at least 10μF output capacitance for stability
- The REF2033A is designed to be stable with capacitive loads up to 10μF

This voltage regulation circuit represents a well-designed power supply system for inverter control and sensing circuits, providing both a stable 3.3V supply for digital and analog components and a precise 1.65V reference for analog signal processing and measurement functions. Attention to filtering, protection, and precision demonstrates professional power electronics design practices aimed at ensuring reliable operation in electrically noisy environments.

4.4 Component Selection Parameters

4.4.1 IGBT Selection (IKP40N65H5XKSA1)

The IKP40N65H5XKSA1 IGBTs used in the power stage require careful selection based on several critical parameters:

1. Voltage Rating: The 650V rating of these IGBTs is selected to provide adequate margin above the DC link voltage. For industrial applications with 400-480VAC input, the DC link can reach approximately 565-680VDC, making 650V IGBTs appropriate with sufficient voltage margin.

2. Current Rating: The current rating must exceed the maximum operational current with appropriate headroom for transient conditions. The specific current rating would be determined based on the inverter's power rating and overload requirements.

3. Switching Characteristics: These IGBTs feature a low collector-emitter saturation voltage (VCE(sat)) to minimize conduction losses during the on-state. The fast switching capability reduces switching losses, which is crucial for efficiency in high-frequency applications.

4. Thermal Considerations: The thermal resistance (junction-to-case) must be low enough to ensure effective heat dissipation. The physical package must allow proper mounting to heatsinks with appropriate thermal interface materials.

4.4.2 Gate Driver IC (UCC21520DW)

The UCC21520DW dual-channel isolated gate driver was selected based on several key parameters: 1. Maximum Gate Driver Supply Voltage: The UCC21520 supports a wide range of supply voltages suitable for driving IGBTs, with specifications showing operation up to 25V, which accommodates the typical +15V/-8V or +15V/0V gate drive requirements for IGBTs.

2. Propagation delay: With a typical propagation delay of 33ns, this driver ensures a rapid response to control signals, which is essential for precise timing in high-frequency switching applications.

3. CMTI (Common-Mode Transient Immunity): The UCC21520 offers high CMTI (typically >100V/ns), which is critical for preventing false triggering during high dv/dt switching events in the power stage.

4. Isolation voltage: The reinforced isolation rating (5.7kVRMS) provides safety separation between the control electronics and the high voltage power stage, meeting the regulatory requirements for industrial equipment.

5. Drive Current Capability: With 4A/6A source/sink capability, the driver can rapidly charge and discharge the IGBT gate capacitance, ensuring fast and clean switching transitions6.

4.4.3 Gate Resistors (16.5Ω and 5.6Ω)

The selection of gate resistors is critical for optimizing switching performance:

1. Turn-on/Turn-off Speed Control: The 16.5Ω resistors in the gate driver output stage and 5.6Ω resistors in the power stage control the charging and discharging rate of the IGBT gate capacitance, directly affecting switching speed.

2. EMI Considerations: Higher gate resistance values reduce dv/dt and di/dt, which decreases electromagnetic interference. The value 16.5Ω probably represents a compromise between switching speed and EMI suppression.

3. Oscillation Damping: The gate resistors are sized to achieve a quality factor (Q) between 0.5 (critically damped) and 1 (under damped) to prevent harmful oscillations in the gate emitter circuit.

4. Power dissipation: The resistors must handle the power dissipation from repeated charging/discharging of the gate capacitance at the switching frequency. This is calculated as $P = C \times V^2 \times f$, where C is the gate capacitance, V is the gate voltage swing, and f is the switching frequency.

4.4.4 Snubber Capacitors (4.7nF)

The 4.7nF snubber capacitors in each IGBT are selected based on:

1. dV/dt Rating: These capacitors must have a dV/dt rating of at least 500-5000 V/μs to handle the rapid voltage transitions during switching.

2. Voltage Rating: The voltage rating must match or exceed the IGBT voltage rating (650V in this case) to ensure reliability during voltage spikes.

3. Capacitance value: The 4.7nF value is determined on the basis of the stray inductance in the circuit and the peak current being switched. For a circuit with 200nH stray inductance switching 2000A with a 1200V IGBT and 564V DC bus, calculations suggest capacitance in the microfarad range, but the lower 4.7nF value indicates this is likely a local snubber for EMI suppression rather than a full DC bus snubber.

4. Dielectric material: Polypropylene is the preferred dielectric material for snubber applications due to its low dissipation factor and good high-frequency characteristics.

4.4.5 Current Sensing Shunt Resistors (0.005Ω)

The ultra-low resistance (0.005Ω) shunt resistors are selected based on:

1. Power dissipation: The low resistance minimizes power losses ($P = I^2R$). For a 70ARMS current, the power dissipation would be approximately 2.45W, which is manageable with proper thermal design.

2. Voltage Signal Level: The value 0.005Ω produces a 50mV signal at 100A, which is within the optimal input range of the isolation amplifier while providing sufficient signal-to-noise ratio5.

3. Temperature coefficient: A low temperature coefficient is essential to maintain measurement accuracy across operating temperature ranges, especially in power electronics where

temperatures can vary significantly.

4. Physical Construction: The four-terminal configuration (Kelvin) separates the current-carrying and sensing paths to improve measurement accuracy by eliminating the effects of connection resistance.

4.4.6 Isolation Amplifiers (AMC1301DWVR and AMC1311DWVR)

These precision isolated amplifiers are selected based on:

1. Isolation Rating: The AMC1301 provides reinforced isolation up to 7070 VPEAK according to DIN EN IEC 60747-17 and UL1577 standards, with a working voltage of up to 1kVRMS, essential for safely measuring signals in high-voltage circuits.

2. Input range: The AMC1301 is optimized for ±250mV inputs, making it ideal for direct connection to low-value shunt resistors, while the AMC1311 has a high-impedance input suitable for voltage divider networks.

3. Common Mode Rejection Ratio: High CMRR is critical for accurate measurements in noisy switching environments, where common mode voltages can be substantial.

4. Accuracy and drift: Low offset voltage, gain error, and temperature drift ensure accurate measurements across operating conditions, which is essential for precise current control in inverter applications.

4.4.7 Voltage Divider Resistors for DC Link Sensing

The high-value resistors ($1M\Omega$ each) in series are selected for the detection of DC link voltages according to the following:

1. Voltage Division Ratio: The six $1M\Omega$ resistors in series with an $11k\Omega$ resistor create a division ratio that scales the high DC bus voltage down to the input range of the isolation amplifier (typically 0-2V).

2. Power dissipation: The high total resistance ($6M\Omega$) minimizes power consumption. With 600VDC across the divider, the power dissipation would be approximately 12mW with a lower resistor $100k\Omega$, representing a good compromise between precision and efficiency.

3. Voltage Rating: Each resistor must withstand its part of the total voltage. Using multiple resistors in series distributes voltage stress, improving reliability in high-voltage applications.

4. Temperature coefficient: Low-temperature coefficient resistors maintain stable division ratios in temperature variations, ensuring accurate voltage measurement under all operating

conditions.

4.4.8 NTC Thermistor Interface Circuit

The NTC thermistor interface for the detection of temperature of the DC link includes:

1. Series Resistors (39Ω): These provide current-limiting protection for the input stage while maintaining signal integrity.

2. Filtering Capacitors (0.01μF): The capacitor filters high-frequency noise that could affect temperature readings, with the value selected to provide adequate filtering without excessive response delay.

3. Reference Resistor Value: Although not explicitly shown in the schematic, NTC thermistor circuits typically use a fixed resistor (often 10$k\Omega$) to create a voltage divider with the thermistor. This value is chosen to be near the thermistor's resistance at the midpoint of the expected temperature range for maximum sensitivity.

4.4.9 Operational Amplifiers (OPA320AIDBVR)

The OPA320AIDBVR precision op-amps are selected based on:

1. Bandwidth: With a 20MHz bandwidth, these op amps can accurately process signals without introducing a significant phase shift at the frequencies present in system.

2. Input Bias Current: The extremely low input bias current (0.9pA typical) ensures minimal loading of high-impedance sources, which is important for accurate signal conditioning.

3. Rail-to-Rail Operation: The rail-to-rail input and output capability maximizes the usable signal range when operating from a single supply, which is important for sensing circuits with limited headroom.

4. Noise performance: Low noise characteristics ensure that the op-amp does not degrade the signal-to-noise ratio of the measurement system, which is critical for accurate current and voltage sensing.

4.4.10 Comparators (TLC372QDRG4)

The TLC372 dual comparators used in the fault detection circuits are selected based on:

1. Supply current: Low supply current (150μA typical per comparator) minimizes power consumption in protection circuits.

2. Response time: The fast response time (200 ns for TTL-level input steps) ensures rapid detection of fault conditions, which is critical to protecting the power stage.

3. Output Current Capability: With 6mA minimum output current capability, the comparators can directly drive fault indication circuits or optocouplers for isolation.

4. Operating Temperature Range: The wide temperature range (-40°C to +125°C for the "Q" version) ensures reliable operation across all expected operating conditions of the power electronics system.

4.4.11 Low-Dropout Regulator (TLV1117-331DCYR)

The TLV1117-331DCYR LDO regulator for the 3.3V supply is selected based on:

1. Input Voltage Range: The wide input voltage range (2.7V to 15V) allows operation from various supply voltages, providing design flexibility.

2. Quiescent Current: The extremely low quiescent current (60μA typical) minimizes power consumption, which is important for efficiency in battery-powered or energy-sensitive applications.

3. Dropout Voltage: The low dropout voltage (typically 1.2V at 100mA) ensures that regulation can be maintained even when the input voltage approaches the output voltage.

4. Output Current Capability: The 800mA output current capability is sufficient to power the isolation amplifiers and signal conditioning circuits in the sensing system.

4.4.12 Filtering Capacitors

Various filtering capacitors are selected throughout the circuit based on:

1. Capacitance values: Different values (0.1μF, 0.47μF, 4.7μF, etc.) are used to filter different frequency ranges of noise. Smaller values (0.1μF) target high-frequency noise, while larger values (4.7μF) handle lower frequencies and provide energy storage for transient loads.

2. Voltage Rating: The voltage rating must exceed the expected maximum voltage with an appropriate margin. For example, capacitors on the 3.3V rail would typically be rated for at least 6.3V or 10V.

3. Dielectric material: X7R or X5R ceramic capacitors are typically used for decoupling because of their good temperature stability and frequency characteristics. Film capacitors might be used where lower dielectric absorption is required.

4. Physical Placement: Although not a selection parameter per se, these capacitors must

be placed as close as possible to the ICs they are decoupling to minimize loop inductance and maximize effectiveness.

This comprehensive analysis of component selection parameters demonstrates the careful engineering considerations required to design a reliable, efficient, and safe three-phase inverter system with sophisticated sensing and protection capabilities.

4.5 PCB Designing

The PCB layout for this three-phase inverter represents a sophisticated design that carefully balances power handling, signal integrity, thermal management, and EMI/EMC considerations. With the additional information from the ground layer, the power layer, and the layer stack manager, we can provide a more comprehensive analysis of this 4-layer PCB design. 1. Layer

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5
1	Top Layer		Signal	1oz	0.03556mm	
	Dielectric 1	FR-4	Core		1.50368mm	4.8
2	GND		Signal	1oz	0.03556mm	
	Dielectric2	FR-4	Core		0.127mm	4.8
3	PWR		Signal	1oz	0.03556mm	
	Dielectric3	FR-4	Core		0.254mm	4.8
4	Bottom Layer		Signal	1oz	0.03556mm	
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5
	Bottom Overlay		Overlay			

Figure 4.10: Layer Stack Managing and Material Selection

Stack Structure and Material Selection

The layer stack manager reveals a carefully engineered 4-layer PCB with the following structure:

- Top Layer (Layer 1): Signal layer with 1oz copper (0.03556mm thickness)
- Ground Layer (Layer 2): Dedicated ground plane with 1oz copper
- Power Layer (Layer 3): Power distribution plane with 1oz copper
- Bottom Layer (Layer 4): Signal layer with 1oz copper

The dielectric materials between layers are:

- Dielectric 1: FR-4 material with 1.50368mm thickness between top and ground layers
- Dielectric 2: FR-4 material with 0.127mm thickness between ground and power layers
- Dielectric 3: FR-4 material with 0.254mm thickness between the power and bottom layers

This stack-up configuration offers several strategic advantages:

- Controlled Impedance: The consistent dielectric thickness and material (FR-4 with Dk=4.8) enables precise control of trace impedance for signal integrity
- EMI Shielding: The ground plane close to the top layer provides excellent shielding for sensitive signals
- Power Integrity: The thin dielectric (0.127mm) between ground and power layers creates high capacitance that helps filter power supply noise
- Thermal Management: The multiple copper layers help to distribute heat across the board.

2. Design and implementation of ground planes The ground layer image reveals a sophisticated ground plane strategy:

- Split Ground Domains: The ground plane is divided into distinct regions for power ground and signal ground, with controlled connection points
- Ground Islands: Strategic isolation areas create separate ground regions for sensitive analog circuits
- Via Stitching: Numerous vias connect the ground plane to ground pours on other layers, reducing ground impedance
- Thermal Relief: Ground connections to thermal pads use thermal relief patterns to balance solderability with thermal performance
- Ground Fills: The ground plane extends under critical signal paths to provide return current paths with a minimal loop area.

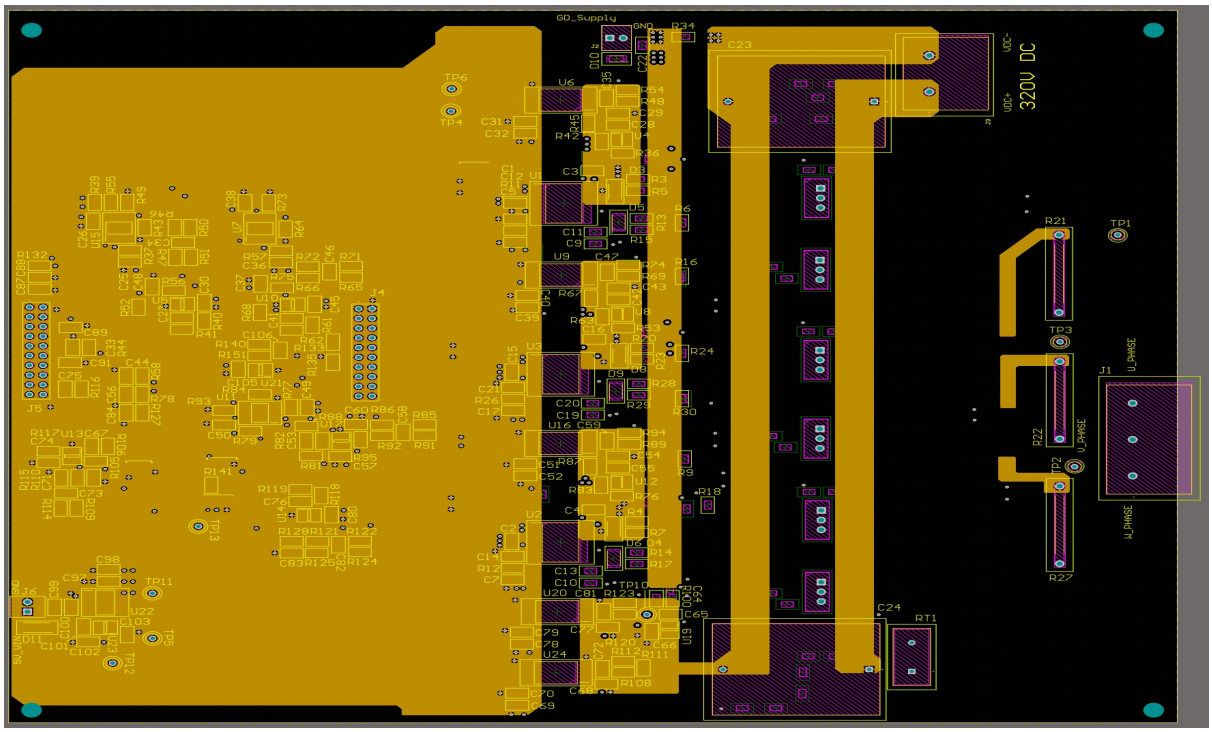


Figure 4.11: Designing ground planes

The ground isolation between power and control sections is particularly noteworthy, with a clear boundary visible in the ground plane that corresponds to the physical division seen in the top layer view.

3. Power Distribution Network The power layer reveals a sophisticated power distribution strategy:

- Multiple Voltage Domains: Separate copper pours for different voltage rails (3.3V, 16V GPS, 5V)
- High Current Paths: Wide copper areas for high-current DC bus connections (320V DC)
- Power Isolation: Clear separation between high-voltage and low-voltage power domains
- Decoupling Support: Power planes positioned to minimize the loop inductance to decoupling capacitors
- Thermal Management: Large copper areas serve dual purposes of current carrying and heat spreading.

The power layer design minimizes voltage drops across the board while maintaining proper isolation between different voltage domains.

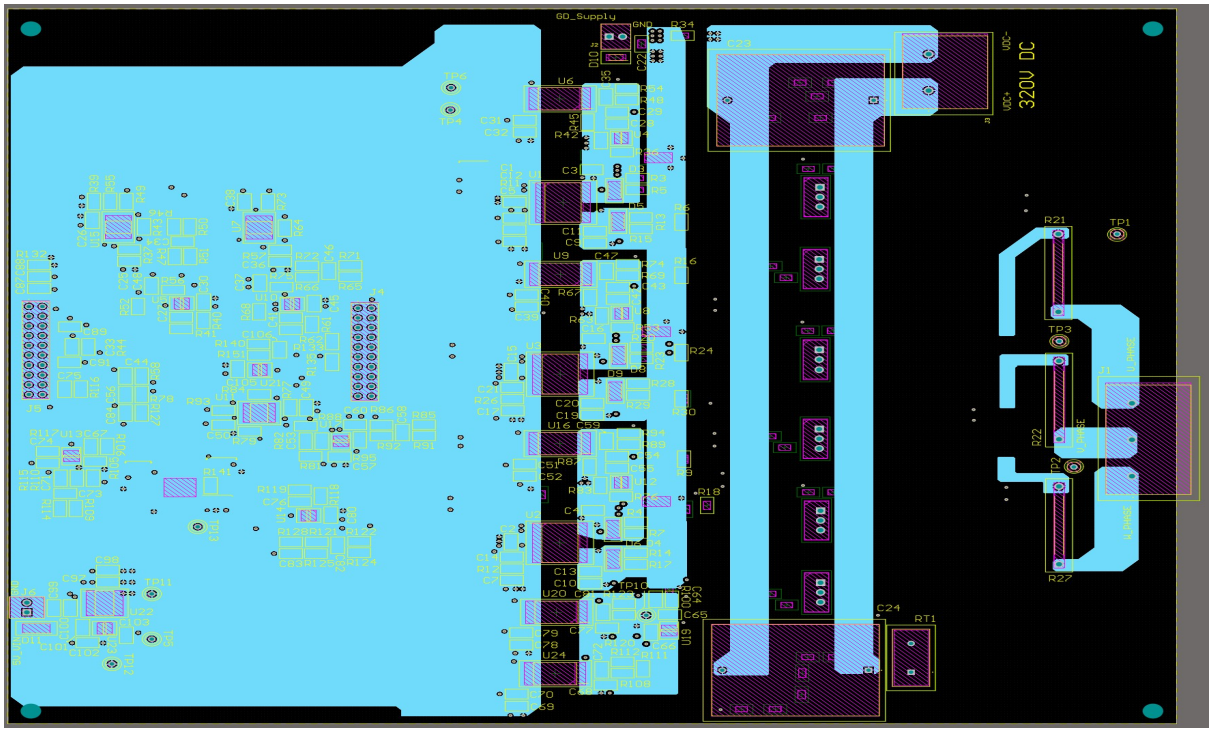


Figure 4.12: Designing power planes

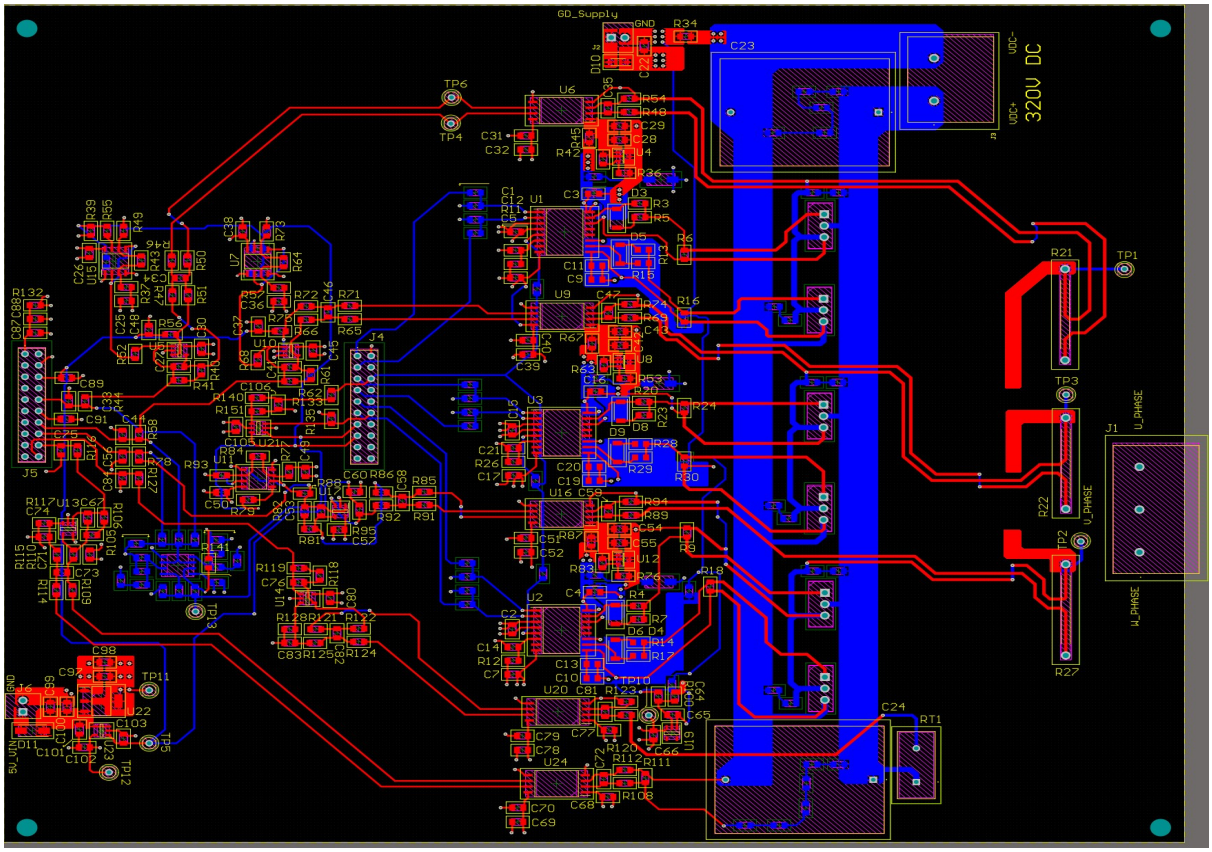


Figure 4.13: Top layer component placement

4. Component Placement Strategy The component placement follows a logical power flow and signal chain approach:

- Power Section Isolation: The high-voltage power components (IGBTs, current sensing resistors) are clearly isolated on the right side of the board
- Gate Driver Proximity: Gate driver ICs (UCC21520DW) are placed close to their respective power transistors to minimize gate loop inductance
- Isolation Barrier: Isolation components (AMC1301/AMC1311) form a clear boundary between high-voltage and low-voltage sections
- Signal Processing Chain: Signal conditioning components (op-amps, comparators) are arranged in logical signal flow order
- Thermal Considerations: Power components have adequate spacing and copper area for heat dissipation.

The test points (TP1, TP3, etc.) are strategically placed near measurement points for easy access during testing and debugging. 5. Implementation of routing guidelines

The PCB routing demonstrates professional power electronics design practices:

- Power Routing: High-current paths use wide traces with minimal length and direct paths
- Signal Integrity: Control signals are routed with consistent trace widths and controlled impedance
- Differential Pairs: Signals like the isolation amplifier outputs are routed as matched-length differential pairs
- Ground References: Signal traces are routed with adjacent ground returns whenever possible
- Layer Transitions: Via placement minimizes signal discontinuities when transitioning between layers.

The routing in both the top and bottom layers shows careful consideration of signal flow, with critical signals given priority routing paths.

6. Implementation of thermal management

Thermal design considerations are evident throughout:

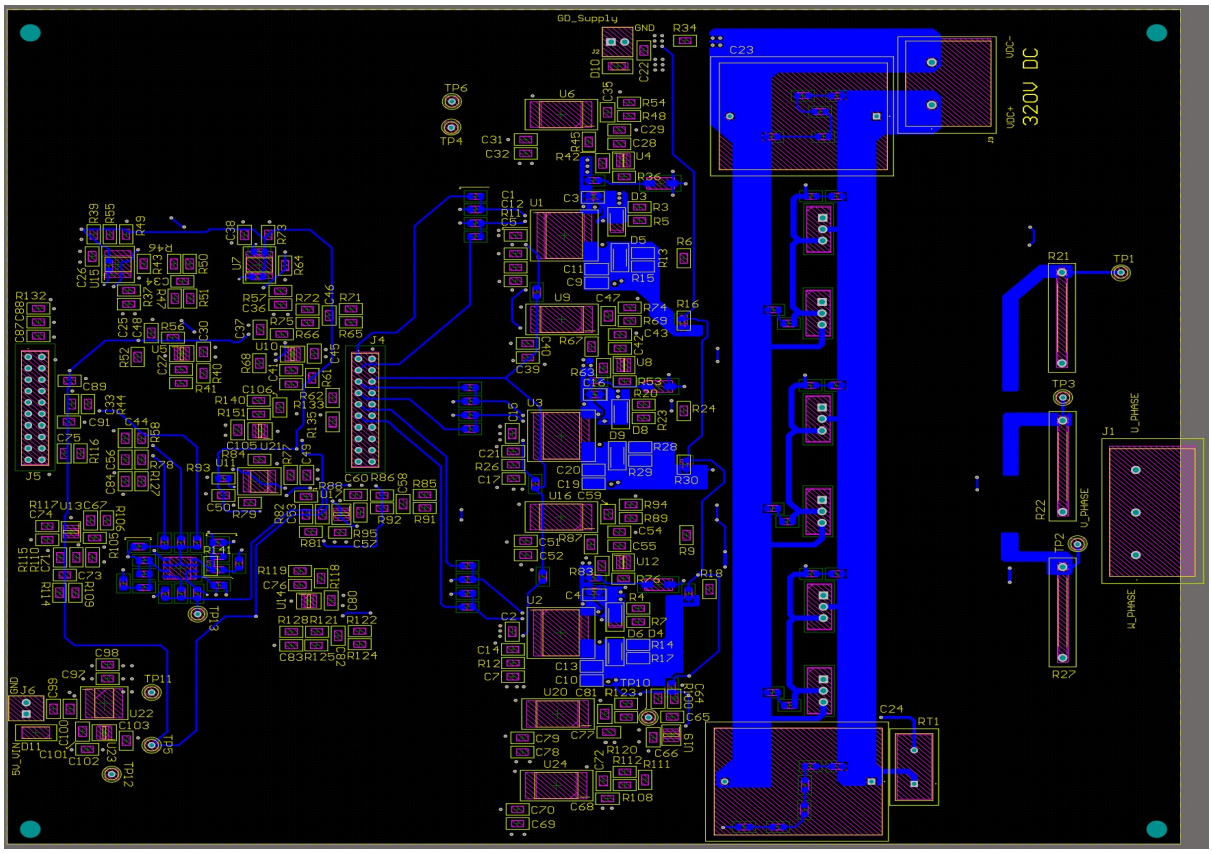


Figure 4.14: Bottom layer component placement

- Copper Pours: Large copper areas on all layers provide heat spreading capability
- Thermal Vias: Arrays of vias under power components transfer heat between layers
- Component Spacing: Adequate spacing between heat-generating components prevents thermal clustering
- Power Dissipation Distribution: Heat-generating components are distributed rather than concentrated
- Thermal Sensing: NTC thermistor placement (RT1) for monitoring critical component temperatures

The 320V DC section has a particularly robust thermal design with extensive copper pour and likely additional cooling considerations.

7. Signal Integrity Features

Signal integrity is maintained through several design techniques.

- Ground-Referenced Routing: Critical signals are routed over continuous ground planes

- Controlled Impedance: Consistent trace widths and layer stackup maintain impedance control
- Minimized Loop Areas: Signal and return paths are kept close to reduce EMI
- Filtering Strategy: Decoupling capacitors placed at strategic locations (C19, C20, etc.)
- Isolation Techniques: Sensitive analog signals are protected from digital and power noise.

The careful routing of the PWM signals (visible in the top layer) demonstrates attention to maintaining the signal integrity for these critical timing signals.

8. EMI/EMC Considerations EMI/EMC design features include:

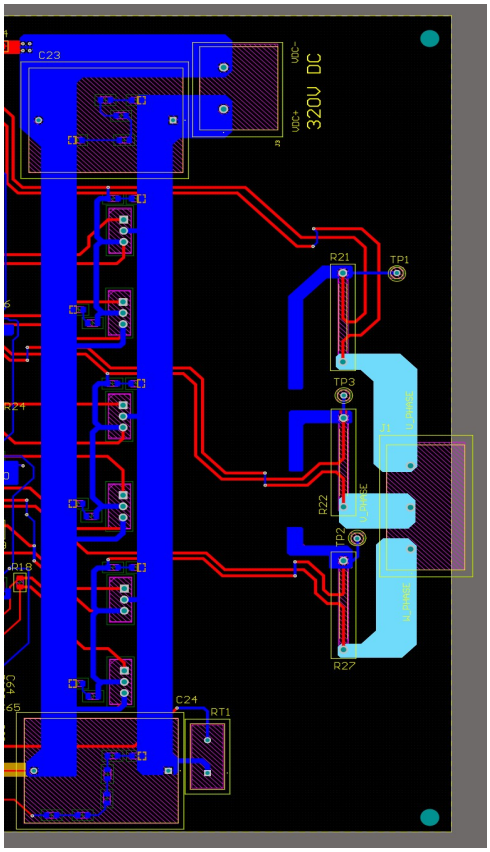


Figure 4.15: Isolating power side

- Ground Plane Shielding: Continuous ground planes reduce radiated emissions
- Loop Area Minimization: Power and signal loops are kept as small as possible
- Filter Components: Strategic placement of filter capacitors and common-mode chokes
- Edge Rate Control: Gate resistors control IGBT switching speed to reduce emissions

- Isolation Barriers: Clear separation between noisy switching circuits and sensitive control circuits

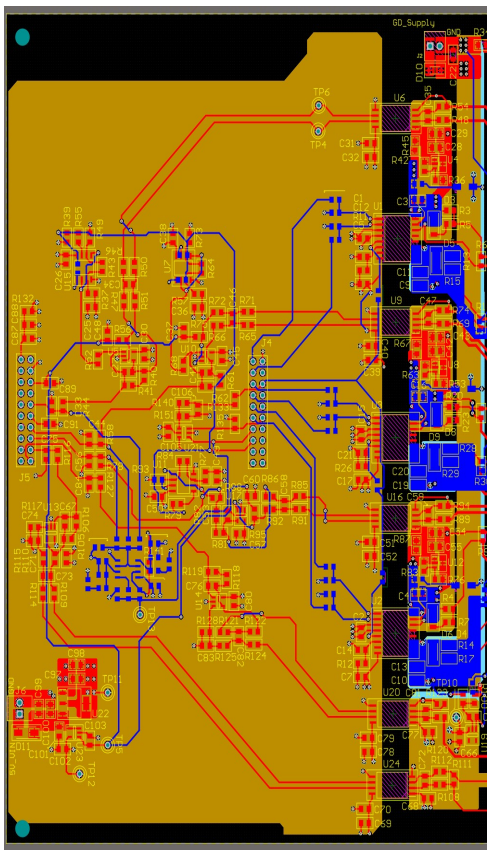


Figure 4.16: Isolating control side

The board layout minimizes both conducted and radiated EMI through careful attention to current paths and loop areas.

9. Clearance and Isolation Implementation

The PCB maintains appropriate clearance for safety and reliability:

- High-Voltage Spacing: Increased spacing around the 320V DC bus connections
- Creepage Distance: Extended surface paths between high-voltage and low-voltage sections
- Reinforced Isolation: The thick dielectric layer (1.50368mm) between top and ground layers enhances isolation
- Safety Barriers: Clear separation between user-accessible connections and high-voltage circuits

- Regulatory Compliance: The spacing appears to comply with the IEC 60950/62368 safety standards.

The isolation between power and control sections is particularly important for safety and noise immunity.

10. Use of EDA tools

The design shows evidence of sophisticated EDA tool usage:

- Layer Stack Management: Precise control of layer thicknesses and materials
- Design Rule Implementation: Consistent application of spacing and width rules
- Copper Pour Management: Sophisticated thermal and ground plane design
- Component Placement Optimization: Strategic placement for thermal, electrical, and manufacturing considerations
- Silkscreen and Documentation: Clear labeling of components, test points, and functional areas

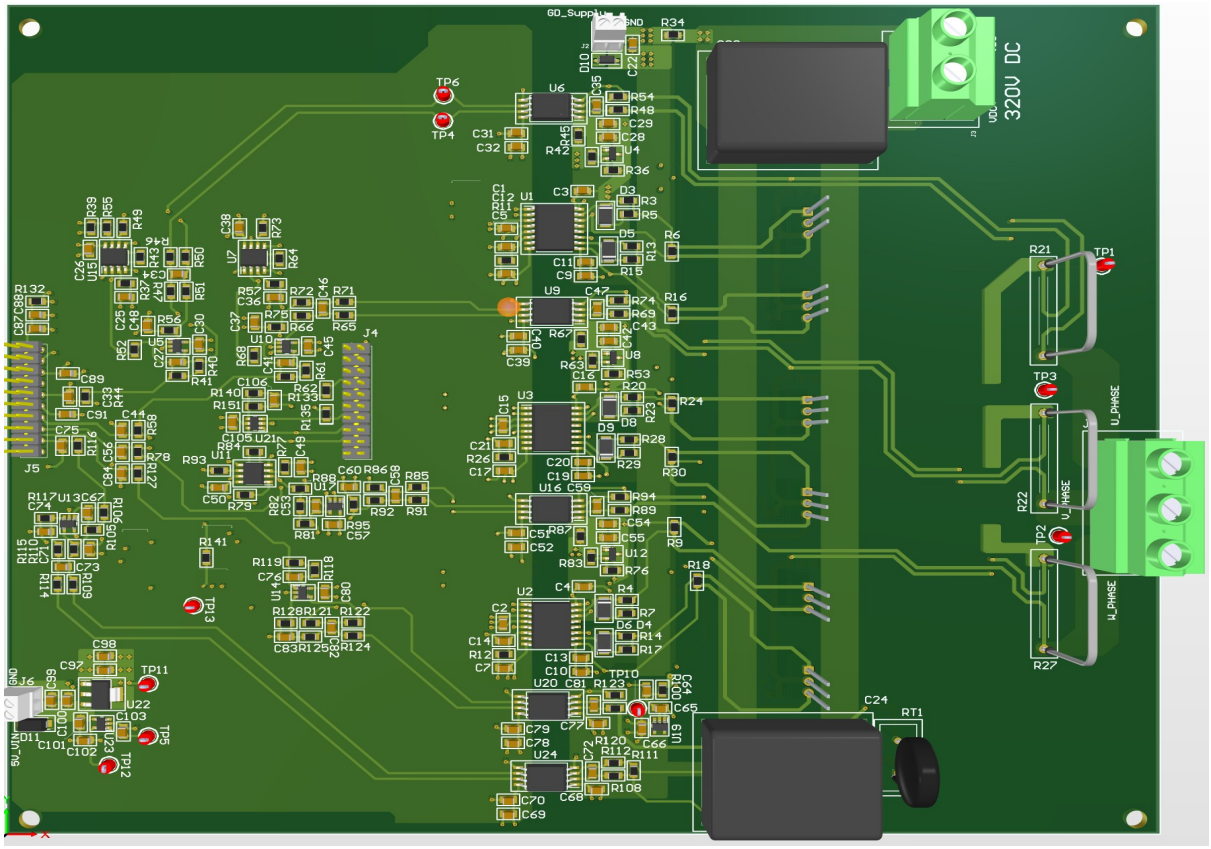


Figure 4.17: Final PCB Top side

The consistency of the design suggests the use of professional EDA tools with specific capabilities for power electronics. This three-phase inverter PCB design represents a professional

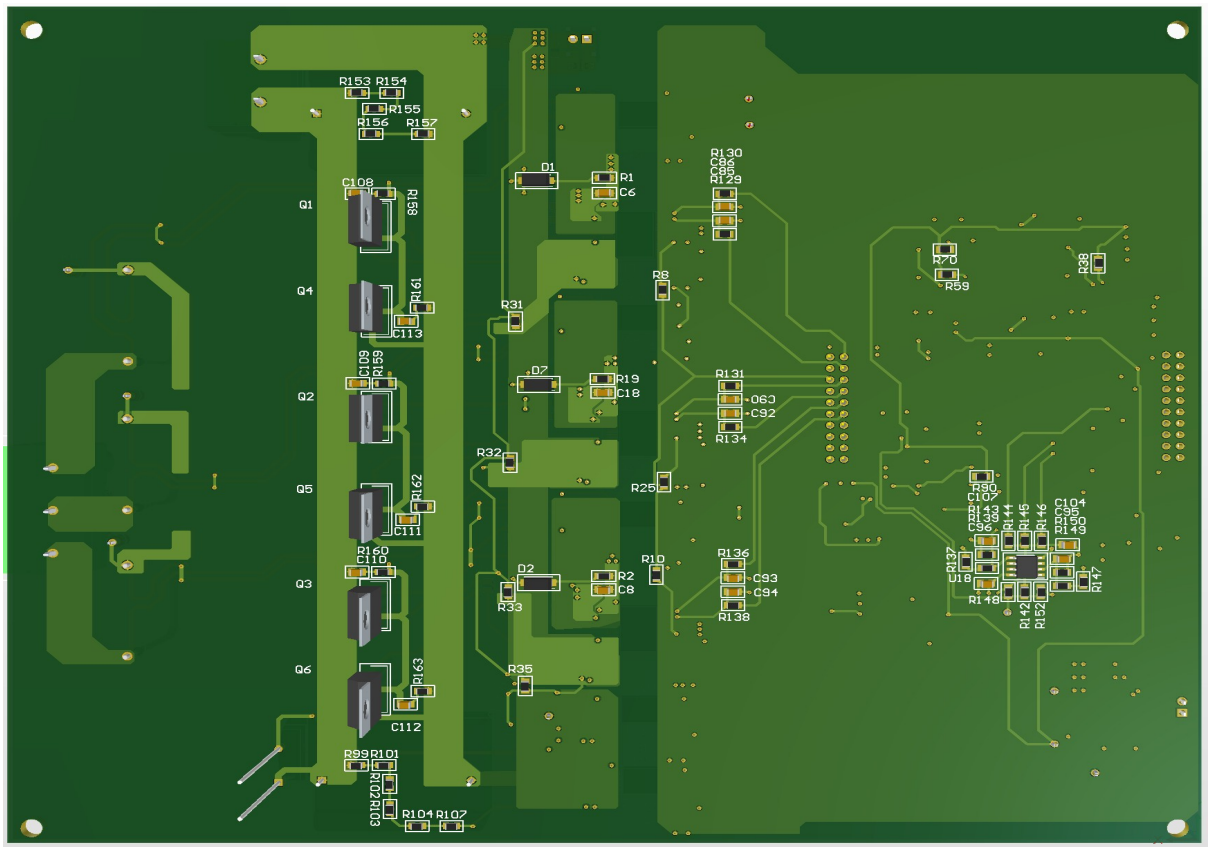


Figure 4.18: Final PCB Bottom side

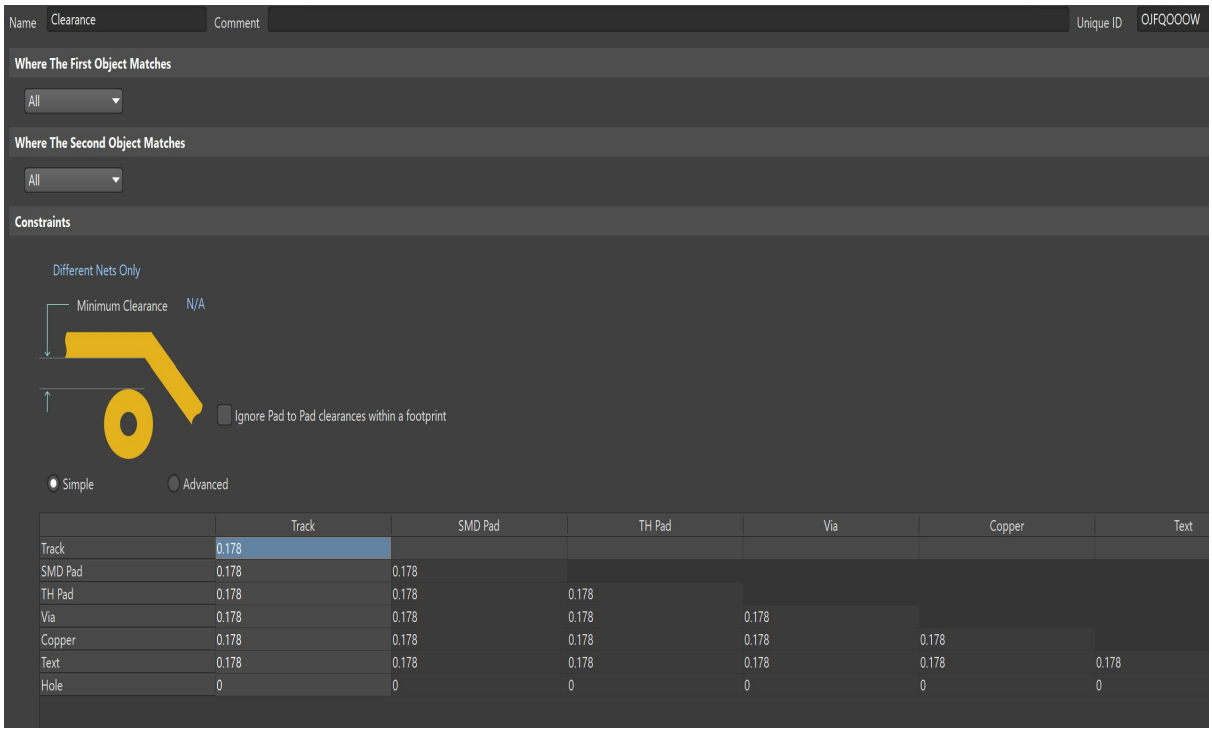
implementation of power electronics design principles, with careful attention to power handling, signal integrity, thermal management, and safety considerations. The four-layer design with dedicated ground and power planes provides an excellent balance of performance, manufacturability, and cost for this application.

4.6 Design Rules

The newly provided design rule files offer valuable insight into the specific constraints and parameters used in the development of the three-phase inverter PCB. These rules demonstrate the professional engineering approach taken to ensure the reliability, manufacturability, and performance of this power electronics design.

1. Clearance Rules The clearance rule configuration reveals meticulous attention to electrical isolation requirements:

- Universal Clearance Standard: A consistent 0.178mm (7 mil) clearance is maintained



	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	0.178					
SMD Pad	0.178	0.178				
TH Pad	0.178	0.178	0.178			
Via	0.178	0.178	0.178	0.178		
Copper	0.178	0.178	0.178	0.178	0.178	
Text	0.178	0.178	0.178	0.178	0.178	0.178
Hole	0	0	0	0	0	0

Figure 4.19: Design rules for clearance

between all PCB objects including tracks, SMD pads, through-hole pads, vias, and copper pours. This value exceeds the minimum 0.1mm (4 mil) clearance recommended by IPC-2221 for general-purpose devices, providing additional safety margin.

- Different Nets Only: The "Different Nets Only" constraint ensures clearance rules are only applied between objects on different electrical networks, which is essential for optimizing board density while maintaining electrical isolation.

- Hole-to-Object Clearance: The 0mm clearance setting for holes indicates that the design relies on the natural isolation provided by the drill hole itself, which is standard practice when the hole is part of the same net as surrounding copper.

This clearance value of 0.178mm represents a careful balance between manufacturing yield, electrical isolation, and board density. For a power electronics application with voltages likely in the 320V DC range, this clearance is supplemented by additional isolation techniques such as conformal coating and the thick dielectric layer (1.50368mm) between the top and ground layers.

2. Power Trace Width Rules The width_power rule configuration demonstrates sophisticated trace width management:

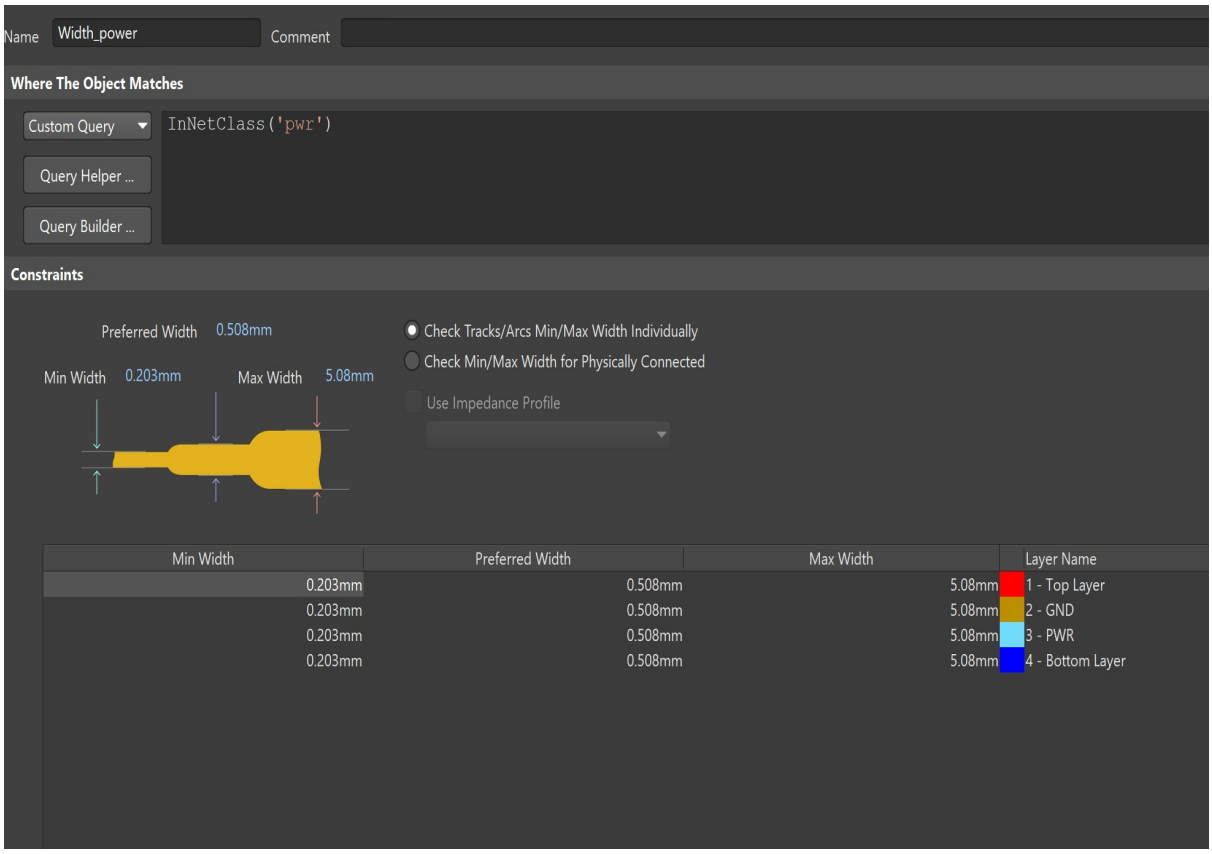


Figure 4.20: Design of trace width rules

- Power Net Classification: The custom query "InNetClass('pwr')" targets specifically designated power nets, ensuring appropriate width rules are applied only to power-carrying traces.
- Width Parameters:
  - Preferred width: 0.508mm (20 mil)
  - Minimum width: 0.203mm (8 mil)
  - Maximum width: 5.08mm (200 mil)
- Layer-Specific Implementation: The rule is applied consistently across all four layers of the PCB, allowing power traces to be routed on any layer while maintaining current-carrying capacity.
- Individual Track/Arc Width Control: The "Check Tracks/Arcs Min/Max Width Individually" option ensures each segment of a power trace meets the width requirements, rather than averaging across connected segments.

These width parameters are scientifically determined based on current-carrying requirements. For power electronics applications, the 0.508mm preferred width for power traces likely supports currents in the 1-2A range with minimal temperature rise, while the maximum 5.08mm width would accommodate much higher currents for the main power paths.

3. Via Design Rules

The routing via configuration shows careful consideration of signal integrity and manufacturing constraints:

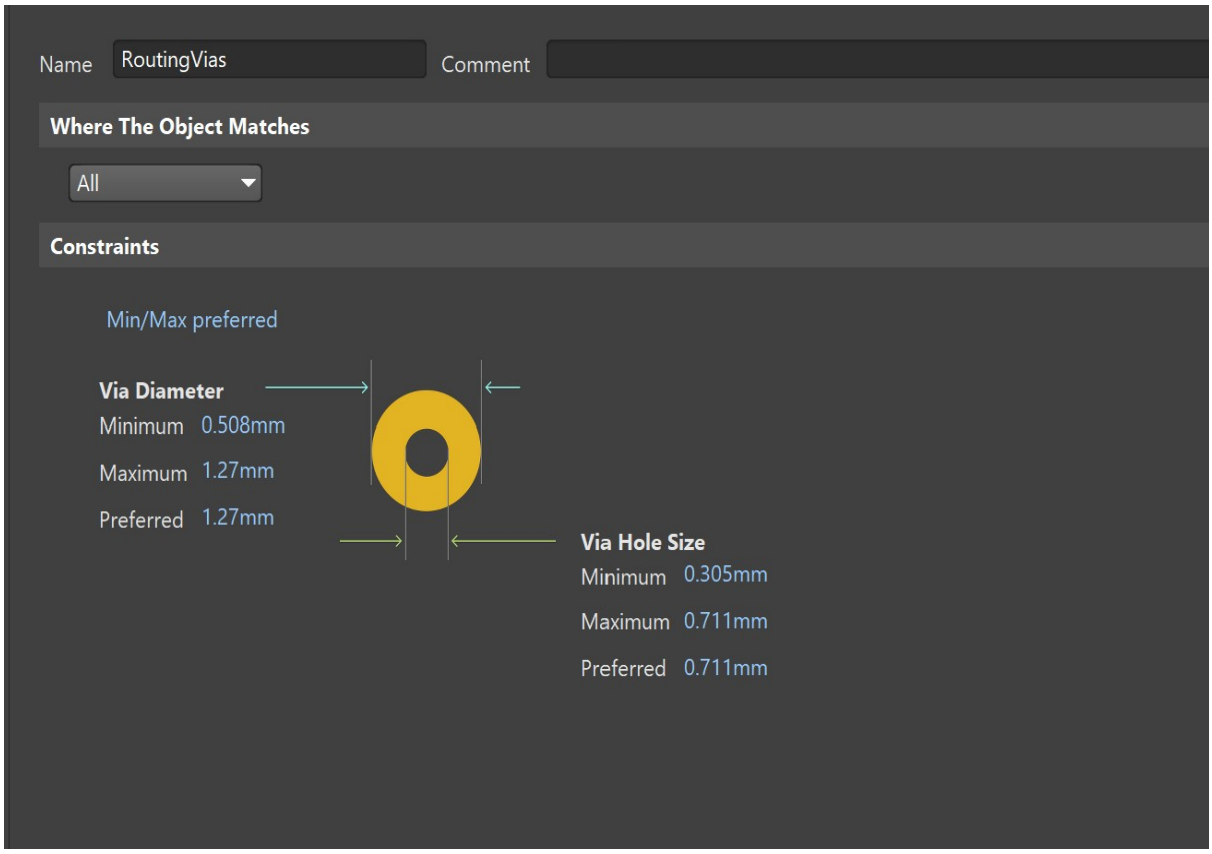


Figure 4.21: Design of via design rules

- Via Diameter Specifications:
  - Minimum: 0.508mm (20 mil)
  - Maximum: 1.27mm (50 mil)
  - Preferred: 1.27mm (50 mil)
- Via Hole Size Parameters:
  - Minimum: 0.305mm (12 mil)

  - Maximum: 0.711mm (28 mil)
  - Preferred: 0.711mm (28 mil)

- Min/Max Preferred Mode: This setting ensures that the vias are sized appropriately for their specific function while maintaining manufacturability.
  - The relatively large via dimensions are appropriate for a power electronics design where:
  - Larger vias reduce resistance and improve thermal performance
  - The 0.305mm minimum hole size ensures reliable plating during manufacturing
  - The 0.711mm preferred hole size accommodates higher current flow between layers
  - The 1.27mm via diameter provides sufficient annular ring (approximately 0.28mm) around the hole, exceeding IPC standards for Class 2 electronics

These via specifications are particularly important for thermal vias under power components and for carrying power between layers with minimal resistance.

4. Component Clearance Rules

The component clearance configuration demonstrates attention to assembly and thermal requirements:

- Vertical clearance: A specified minimum vertical clearance of 0.254mm (10 mil) ensures adequate separation between components mounted on opposite sides of the board.
- Horizontal Clearance: A minimum horizontal clearance of 0.254mm (10 mil) between components ensures sufficient space for assembly processes and thermal management.
- Specified mode: The use of a "Specified" mode rather than "Infinite" indicates that the design has precise clearance requirements rather than arbitrary separation.

These component clearance values are aligned with industry standards for manufacturability while addressing the critical thermal considerations in power electronics. The 0.254mm spacing helps prevent component interference during reflow soldering and provides some thermal isolation between heat-generating components.

5. Integration of Design Rules in PCB Implementation

These design rules work together to create a robust power electronics PCB:

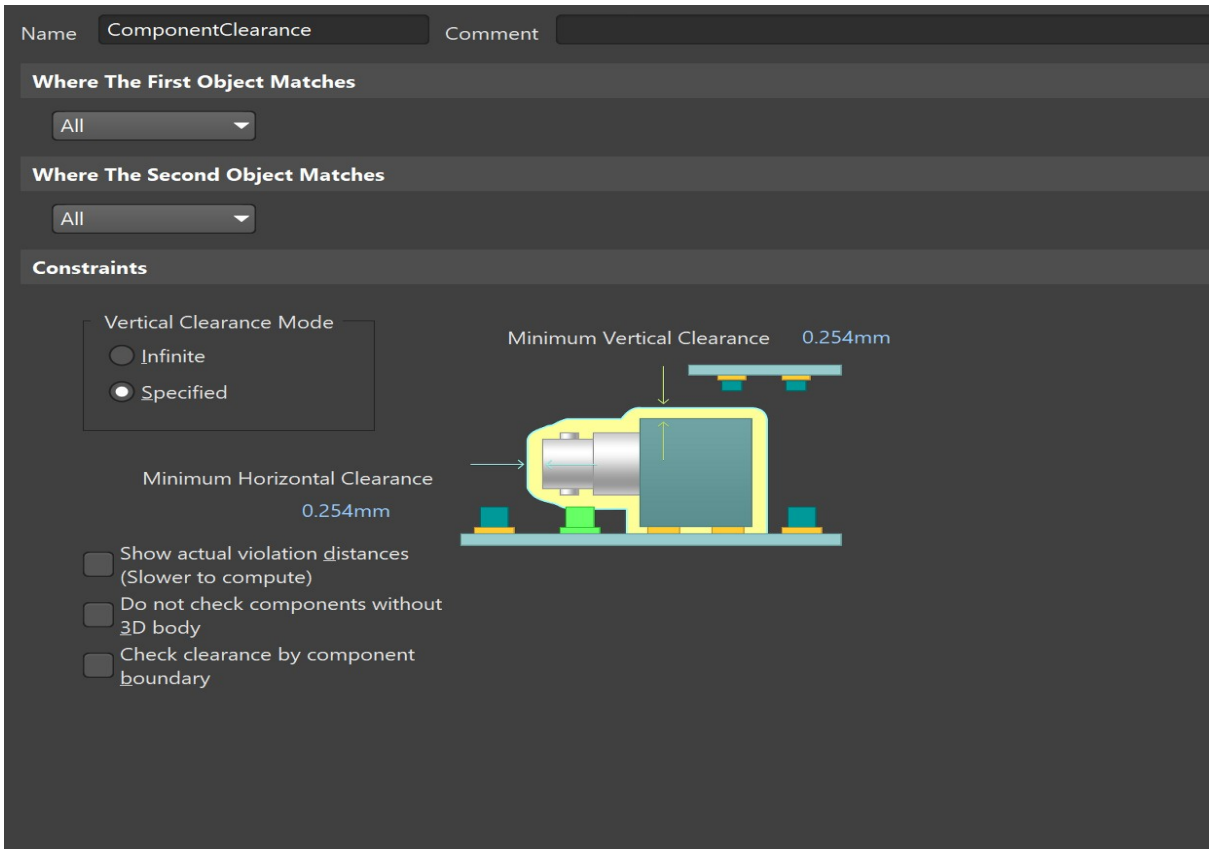


Figure 4.22: Design of component clearance rules

- Power handling capacity: The combination of wide power traces (up to 5.08mm) and large vias (1.27mm) ensures adequate current-carrying capacity for the inverter's power stage.
- Signal Integrity: The consistent 0.178mm clearance prevents crosstalk between sensitive control signals and noisy switching nodes.
- Thermal Management: Component clearances of 0.254mm provide space for heat dissipation, while large vias facilitate heat transfer between layers.
- Manufacturing Reliability: All clearance and width parameters exceed the minimum manufacturing capabilities, ensuring high yield during production.
- Safety Compliance: The combination of clearance rules, stacking of layers, and component placement ensures compliance with safety standards for power electronics equipment.

The implementation of these design rules is evident in the PCB layout, where power components are adequately spaced, control signals are properly isolated, and thermal management is

addressed through strategic component placement and copper distribution. These design rules represent industry best practices for power electronics design, ensuring a reliable, manufacturable, and high-performance three-phase inverter system capable of handling the electrical, thermal, and safety requirements of industrial applications.

4.7 Control System Architecture

The block diagram illustrates a comprehensive control system for a three-phase standalone inverter designed to operate with balanced loads. This sophisticated control architecture represents a modern approach to power conversion systems used in applications such as uninterruptible power supplies (UPS), microgrids, and renewable energy systems operating in island mode. The system employs a dual-loop control strategy with cascaded voltage and current con-

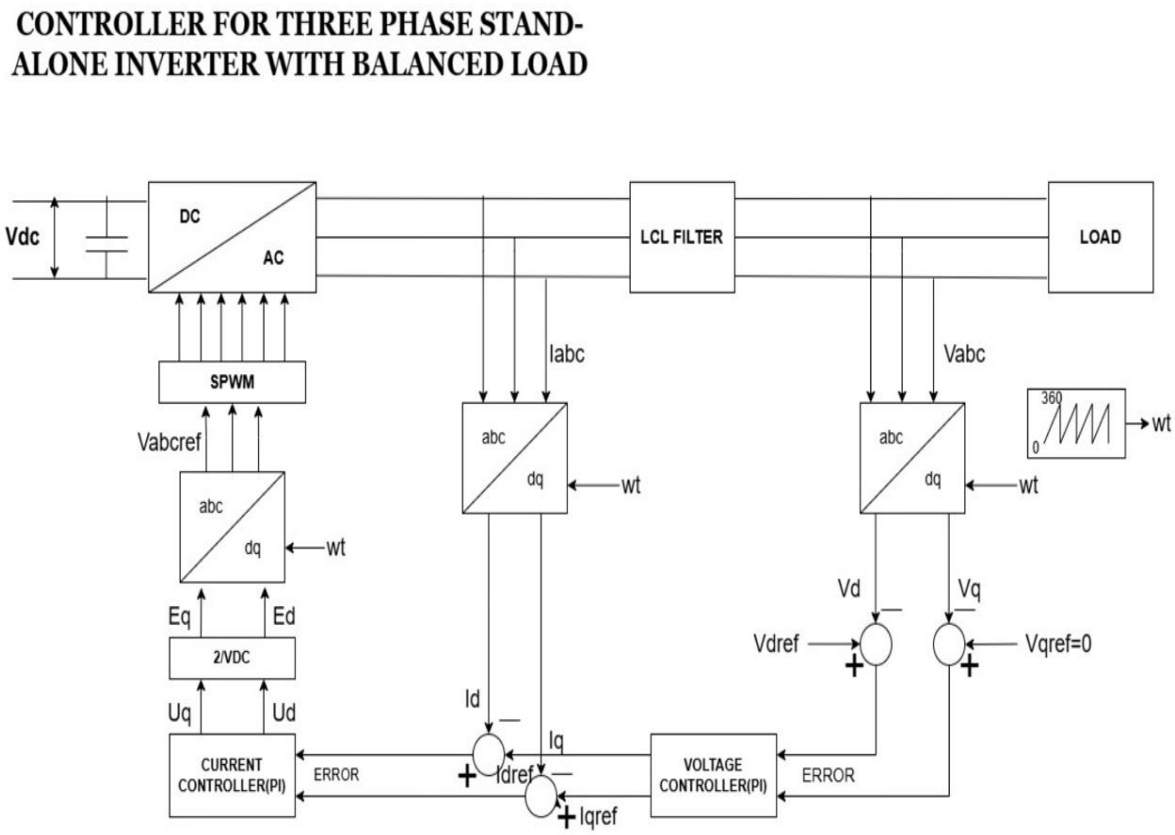


Figure 4.23: Block diagram of PI Controller

trollers operating in the synchronous reference frame (dq coordinates). This approach allows for decoupled control of active and reactive power components, providing precise regulation of the output voltage magnitude and frequency regardless of load variations. The control structure begins with a DC source that feeds a three-phase inverter, followed by an LCL filter to attenuate

switching harmonics, ultimately delivering clean sinusoidal power to the balanced three-phase load. What distinguishes this control system is its implementation of coordinate transformations (abc-to-dq and dq-to-abc) that simplify the control problem by converting time-varying AC quantities into DC-like quantities in a rotating reference frame. This transformation enables the use of conventional PI controllers to achieve zero steady-state error and robust performance under varying operating conditions.

1. Power Stage Components

The power flow begins on the left side with a DC source (Vdc) that supplies energy to the inverter. This DC voltage is typically provided by batteries, solar panels with DC-DC converters, or a rectified AC source with filtering.

The DC-AC conversion block represents the three-phase inverter power stage, which consists of six semiconductor switches (typically IGBTs or MOSFETs) arranged in three half-bridge configurations. Each phase leg contains two switches that operate complementarily with appropriate dead time to prevent shoot-through conditions.

The LCL filter following the inverter serves to attenuate the high-frequency switching components from the PWM process. This filter typically consists of:

- Inverter-side inductors to smooth the output current
- Capacitors connected in star or delta configuration
- Grid-side inductors to attenuate higher harmonics and limit grid-side current ripple

The LOAD block represents the three-phase balanced load, which could be resistive, inductive, or a combination depending on the application (motors, heating elements, or other three-phase equipment).

2. Measurement and Feedback Systems

The system incorporates two measurement points:

- Current measurement (Iabc) after the inverter output
- Voltage measurement (Vabc) at the load terminals

These measurements are transformed from the three-phase stationary reference frame (abc) to the synchronously rotating reference frame (dq) using coordinate transformation blocks. This transformation simplifies control by converting AC quantities to DC-like quantities, enabling the use of conventional PI controllers.

3. Reference Generation and Synchronization

The angular reference (wt) is generated by a sawtooth waveform generator that produces a signal ramping from 0 to 360 degrees. This provides the synchronization angle for all coordinate transformations, ensuring that the control system operates in a properly aligned reference frame. The voltage references are set with Vdref as the desired magnitude of the output voltage, while Vqref is set to zero to align the reference frame with the d-axis, simplifying the control structure.

4. Cascaded Control Structure

The control system implements a cascaded structure with:

- Voltage Controller (PI): The outer loop compares the measured load voltages (Vd, Vq) with their references (Vdref, Vqref=0). The error signals drive PI controllers that generate current references (Idref, Iqref) for the inner loop.
- Current Controller (PI): The inner loop compares measured currents (Id, Iq) with the references from the voltage controller. The resulting error signals drive another set of PI controllers that generate the control signals (Ud, Uq).
- Feed-Forward Block (2/VDC): This block scales the controller outputs based on the DC bus voltage, providing compensation for DC voltage variations and improving dynamic response.
- Coordinate Transformation (dq to abc): The controller outputs (Ed, Eq) are transformed back to three-phase quantities (Vabcref) to generate the modulation signals for the SPWM generator.

5. SPWM Generation

The Sinusoidal Pulse Width Modulation (SPWM) block takes the reference signals in three phases and generates six switching signals for the inverter power semiconductors. This typically involves comparing sinusoidal reference signals with a high-frequency triangular carrier to create the appropriate duty cycles for each switch.

6. Control System Operation

The complete control loop operates as follows:

- Load voltages are measured and transformed to the dq domain
- Voltage errors drive the outer PI controllers to generate current references

- Currents are measured and transformed to the dq domain
- Current errors drive the inner PI controllers to generate control signals
- Control signals are scaled by the DC bus voltage and transformed back to abc domain
- SPWM generator creates switching signals for the inverter
- Inverter converts DC to three-phase AC
- LCL filter smooths the output waveforms
- Balanced load receives regulated three-phase voltage

This dual-loop control structure provides excellent voltage regulation, fast dynamic response, disturbance rejection, and inherent current limiting capabilities, making it suitable for standalone applications such as UPS systems, microgrids, or off-grid renewable energy systems.

5 EXPERIMENTS & SIMULATIONS

The provided MATLAB Simulink model represents a comprehensive implementation of a three-phase grid-connected voltage source inverter (VSI) with PI controller-based feedback control. This simulation demonstrates the application of the synchronous reference frame theory for precise control of the three-phase AC output. The simulation consists of two main

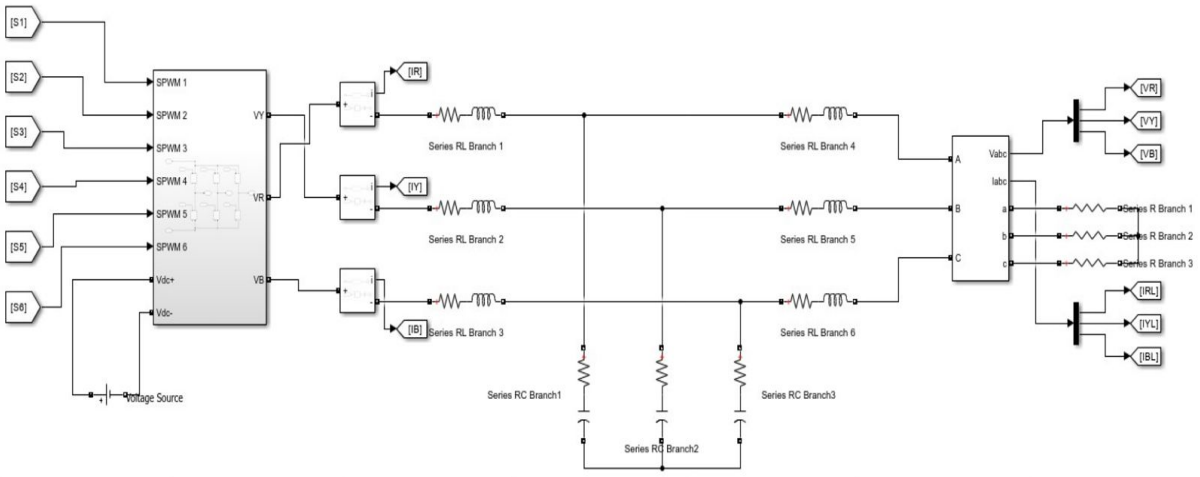


Figure 5.1: Matlab simulink model of three-phase inverter

sections: The power circuit: A three-phase inverter with DC source, switching devices, and output filters The control circuit: A sophisticated control system that implements synchronous reference frame control with PI controllers

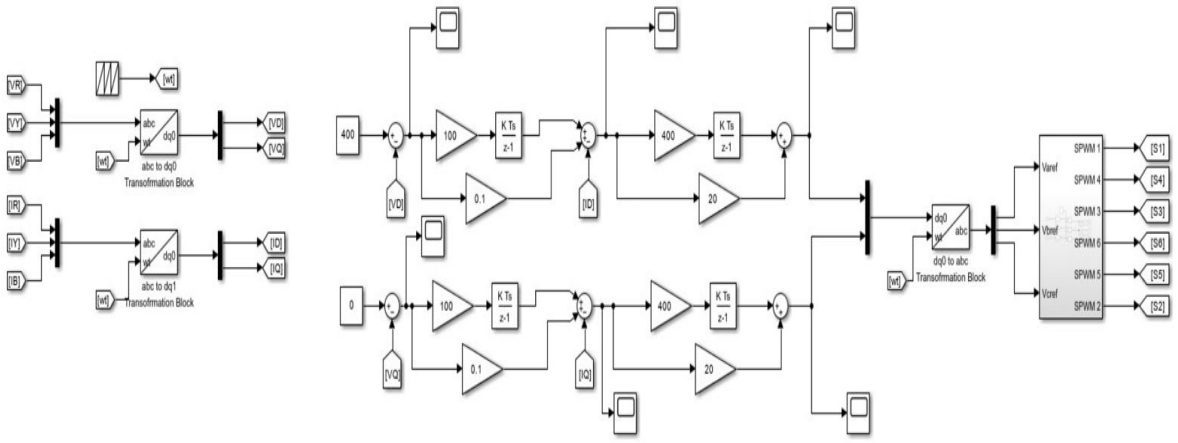


Figure 5.2: Matlab simulink model of control circuit

1. Power Circuit Architecture

The power circuit includes:

- DC Voltage Source: Provides the input power to the inverter

- Three-Phase Inverter: Represented by the "Inverter System" block with six PWM inputs (SPWM 1-6) controlling the switching devices
- Output Filter: Series RL branches (1-6) forming an LCL filter configuration to reduce harmonics
- Three-Phase Measurement Block: Measures output voltages and currents at the connection point

The inverter uses six switching signals to control the three half-bridge legs (one for each phase). Each leg consists of two switches that operate in a complementary manner to produce the desired AC waveform.

2. Control System Implementation

The control system implements a dual-loop control structure based on synchronous reference frame theory:

1. **Three-Phase Voltage/Current Measurement:** The system measures three-phase voltages (V_{VR}, V_{VY}, V_{VB}) and currents (I_{VR}, I_{VY}, I_{VB}).
2. **ABC to $\alpha\beta 0$ Transformation:** The measured three-phase quantities are transformed to the stationary reference frame ($\alpha\beta 0$) using:

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} = \begin{bmatrix} 1 & -\frac{3}{3} & -\frac{3}{3} \\ \frac{2}{3} & \frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}$$

3. $\alpha\beta 0$ **to** $dq0$ **Transformation:** The stationary frame quantities are further transformed to the synchronously rotating reference frame ($dq0$) using:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix}$$

where θ is the grid voltage angle determined by the Phase-Locked Loop (PLL).

3. Phase locked loop (PLL)

The PLL is implemented to synchronize the control system with the grid voltage:

- The $\alpha\beta$ voltage components are fed to the PLL block
- The PLL uses PI controllers with gains of 100 and K·Ts/(z-1) transfer functions to track the grid angle
- The output provides the synchronized phase angle used for dq transformations

4. Current Control Loop

The inner current control loop:

- Error calculation: The measured d-q currents (Id, Iq) are compared with reference values to generate error signals
- PI Controllers: The errors are processed through PI controllers with proportional gain of 400 and integral gain implemented through K·Ts/(z-1) transfer functions
- Cross-Coupling Compensation: The controller includes decoupling terms (20·Iq and 20·Id) to account for the cross-coupling effect between the d and q axes.

The PI controller parameters are carefully selected based on the system parameters:

- Proportional gain: 400
- Integral gain: Implemented through discrete transfer functions
- Decoupling gain: 20 (representing 2πfL, where L = 11.7mH and f = 50Hz)

5. Voltage Control Loop The outer voltage control loop:

- Reference Generation: Generates the reference currents for the current control loop
- PI Controllers: Process voltage errors to generate current references
- Feedforward Terms: Include feedforward terms to improve dynamic response

6. PWM Generation

The final stage converts the control output back to three-phase PWM signals:

- dqθ to $\alpha\beta\theta$ Transformation: Converts the control signals from dqθ back to $\alpha\beta$
- $\alpha\beta\theta$ to ABC Transformation: Converts $\alpha\beta\theta$ signals to three-phase reference signals
- SPWM Generator: Generates six PWM signals (SPWM 1-6) for inverter switches

7. Filter Design Considerations

The LCL filter is designed with:

- Series RL branches representing the inverter-side and grid-side inductors
- Series RC branches representing the filter capacitors
- Values selected to provide adequate filtering while maintaining system stability

8. Selection of control parameters

The PI controller parameters are selected based on:

- System Time Constants: Related to the L/R ratio of the filter
- Desired Bandwidth: Typically 1/10 of the switching frequency
- Stability Margins: Ensuring adequate phase and gain margins
- Decoupling Requirements: The cross-coupling terms (20·Id and 20·Iq) are calculated as ωL

The proportional gain (400) and the integral gain (implemented through K·Ts/(z-1)) provide a balance between response speed and stability. This three-phase inverter simulation with PI control represents a sophisticated implementation of modern power electronics control theory, suitable for applications in renewable energy integration, motor drives, and grid-connected power conversion systems.

5.1 Analysis Analysis of Three-Phase Inverter Simulation Waveforms

The provided waveforms represent the output results of the three-phase inverter simulation with PI control implementation. These graphs demonstrate the performance of the control system and the quality of the output waveforms.

1. Three-Phase Current Waveforms

The figure 5.3 shows the three-phase output currents (Ir, Ib, Iy):

- The three sinusoidal waveforms are displaced by 120° from each other, confirming proper three-phase operation
- The amplitude appears to be approximately ±6A peak, indicating consistent current control across all phases

- The waveforms show excellent sinusoidal quality with minimal distortion, demonstrating effective filtering and control
- The time scale spans from approximately 0.15s to 0.25s, showing steady-state operation
- The frequency appears to be 50Hz (5 complete cycles in 0.1s), which is the standard grid frequency

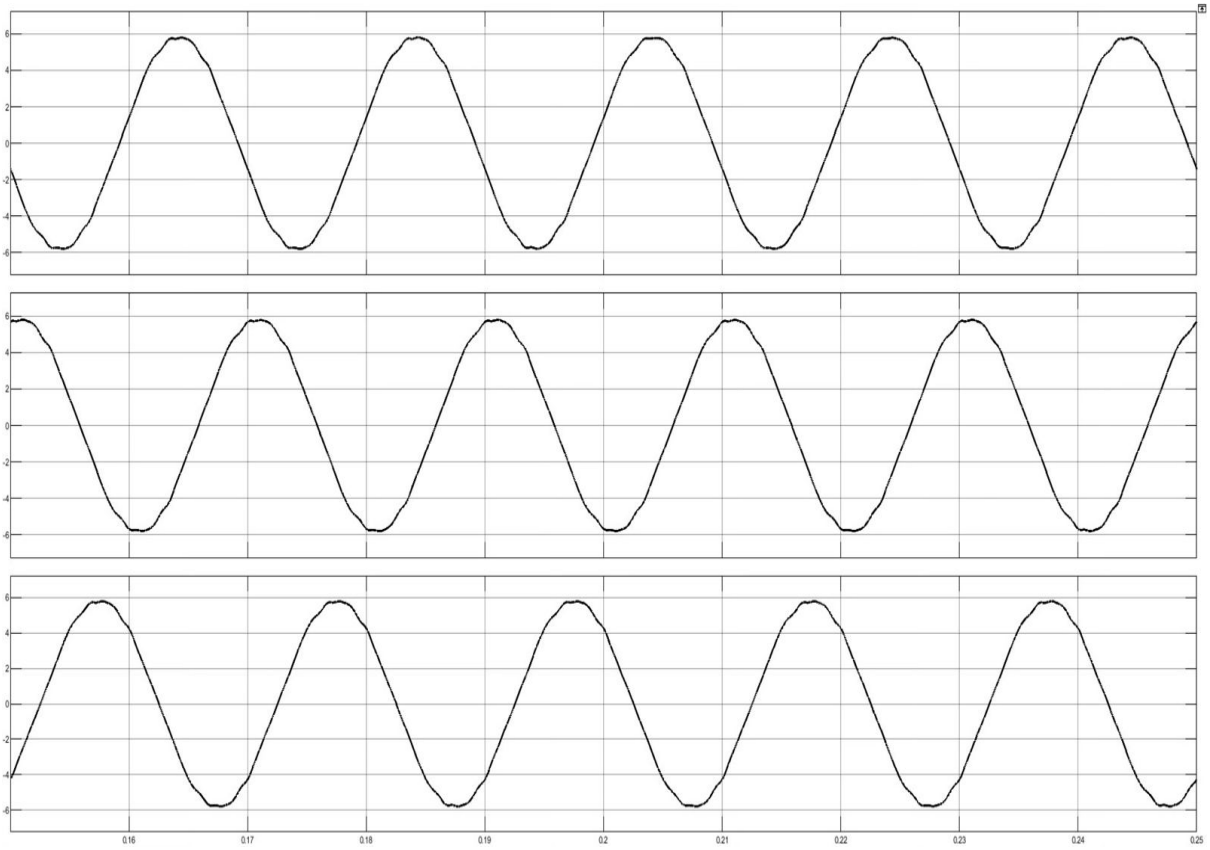


Figure 5.3: The three phase output currents Ir, Ib and Iy

These current waveforms indicate that the current control loop is functioning correctly, maintaining balanced three-phase currents with proper phase relationships.

2. Three-Phase Voltage Waveforms

The Figure 5.4 displays the three-phase output voltages:

- The sinusoidal waveforms maintain precise 120° phase displacement
- The amplitude is approximately ±600V peak (around 424V RMS), which is typical for a three-phase 400V system
- The waveforms exhibit excellent sinusoidal quality, indicating proper filtering of PWM switching harmonics

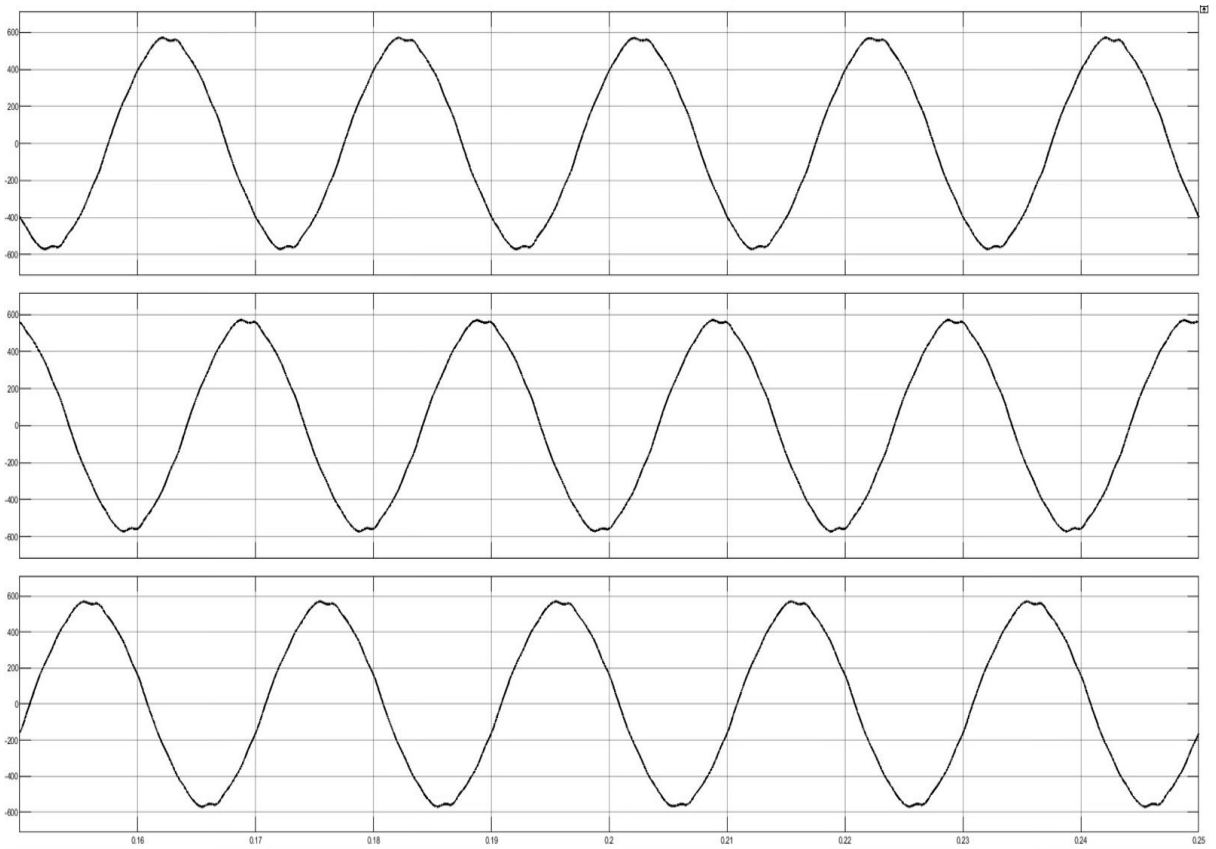


Figure 5.4: The three phase output Voltage Vr, Vb and Vy

- The time scale matches the current waveforms (0.15s to 0.25s)
- The frequency is 50Hz, synchronized with the current waveforms

The quality of these voltage waveforms demonstrates that the voltage control loop effectively regulates the output voltage magnitude and waveform shape.

3. Controller Performance Waveforms

Figures 5.5 and 5.6 show the controller performance:

- The figure 5.5 shows a flat line at approximately zero, which likely represents the q-axis current controller PI output in steady state, indicating that the controller has reached equilibrium with minimal error
- The figure 5.6 shows small fluctuations in the 10÷11 range, which represents the q-axis voltage controller PI output error signal. The extremely small magnitude indicates excellent steady-state performance with negligible error.

These controller output waveforms confirm that:

- The PI controllers have successfully reached steady state

Figure 5.5: The current controller PI output waveform(q-axis)

- The control system is maintaining the desired reference values with minimal error
- The decoupling between d and q axes is effective, as evidenced by the stable controller outputs

Figure 5. 7 shows the output of the PI output of the voltage controller d-axis over a simulation time of approximately 0.23 seconds. This waveform exhibits several key characteristics:

- The signal maintains a nearly constant value around 30-40 units after initial startup
- There is minimal oscillation or ripple, indicating excellent steady-state performance
- The horizontal scale spans from 0 to 0.23 seconds, capturing both the initial transient and steady-state operation
- The vertical scale ranges from approximately -600 to 600, though the signal uses only a small portion of this range

This waveform demonstrates that the voltage controller has reached a stable operating point with minimal error. The flat and steady nature of the signal indicates that the PI controller is maintaining the desired reference voltage d-axis with high precision.

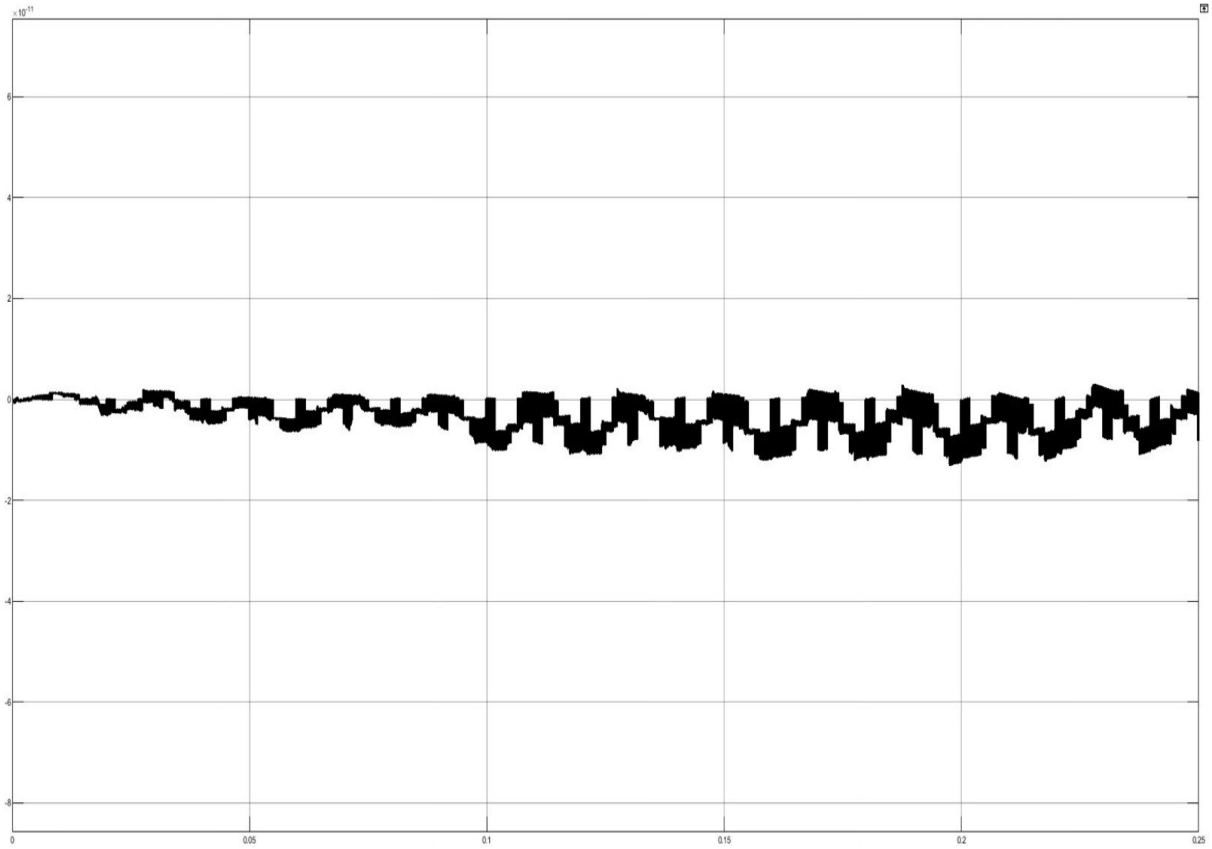


Figure 5.6: The voltage controller PI output waveform(q-axis)

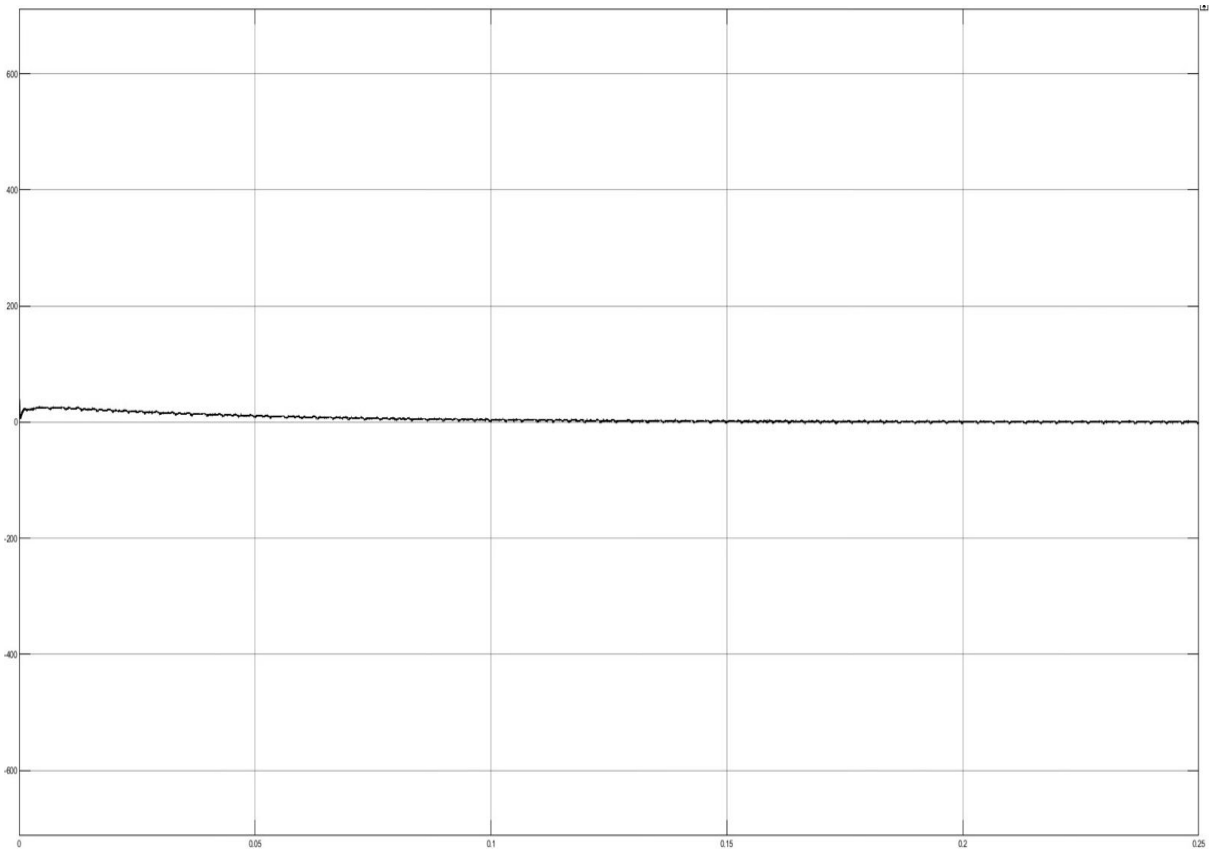


Figure 5.7: The voltage controller PI output waveform (d-axis)

The Figure 5.8 waveform displays the PI output from the current controller d-axis over the same time period. This signal shows:

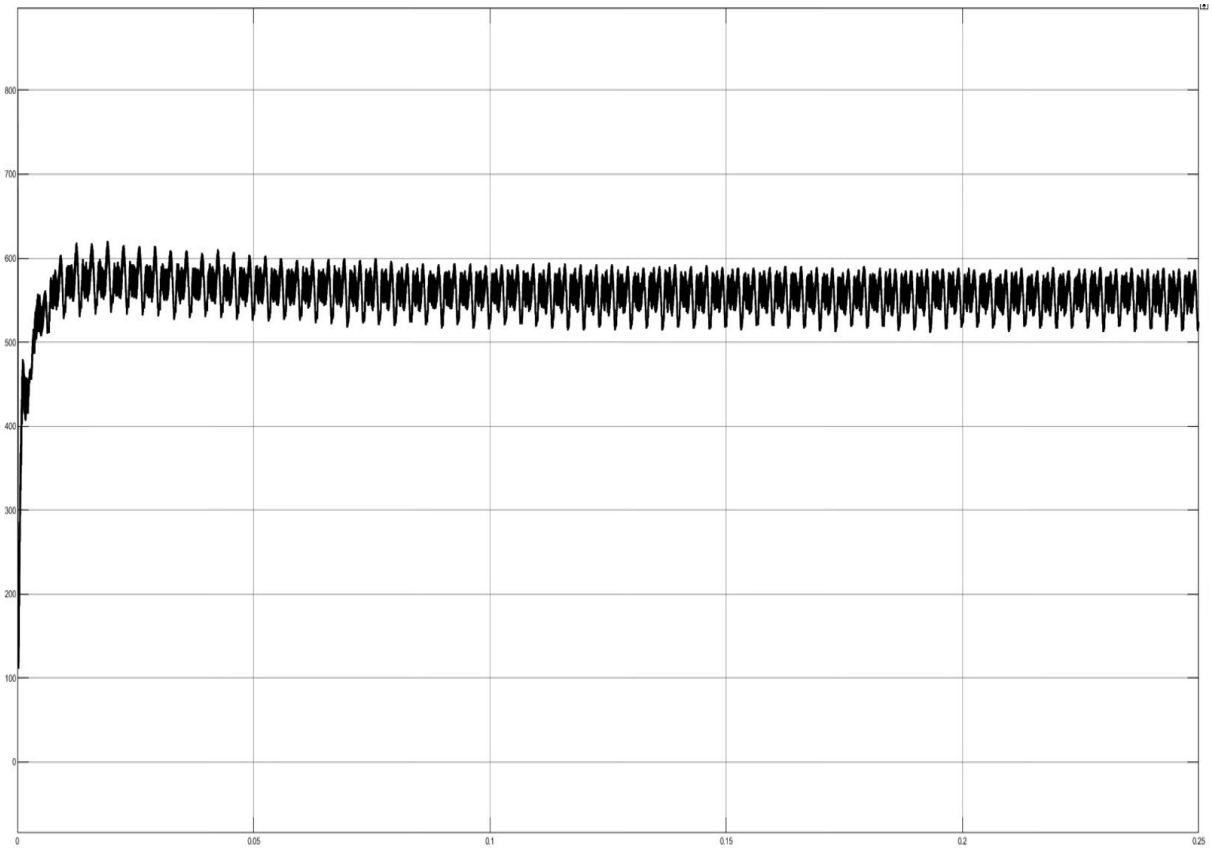


Figure 5.8: The current controller PI output waveform (d-axis)

- An initial transient response during startup (0-0.02s), where the value rises rapidly from around 100V to approximately 550V
- A steady-state operation with consistent high-frequency ripple between approximately 550-600V
- Regular oscillations that maintain a consistent pattern throughout steady-state operation

The frequency of the ripple appears to be related to the inverter switching frequency. The ripple in this waveform is expected and represents the continuous adjustments made by the current controller to maintain the desired current level. The consistent amplitude of these oscillations indicates that the controller is operating properly and maintaining stable operation. The presence of ripple in the current controller output but not in the voltage controller output demonstrates the cascaded control structure, where the inner current loop handles faster dynamics, while the outer voltage loop maintains overall stability. The overall quality of the

waveform shows that the synchronous reference frame control with PI controllers effectively regulates both voltage and current in the three-phase inverter system, producing high-quality sinusoidal output with proper phase relationships and minimal distortion.

5.2 Hardware implementation of Three phase spwm implementation

The below setup shows the hardware implementation of a three-phase sine waveform. The complete hardware set-up for the three-phase SPWM generation is that it includes an FPGA development board (T20Q14414), an RC filtering network for waveform smoothing, and an oscilloscope for real-time waveform analysis. The FPGA is programmed using Efinity software to generate SPWM signals, which are then processed by the RC network to produce smooth sine waves for three phases. The oscilloscope screen displays the waveforms for phases A

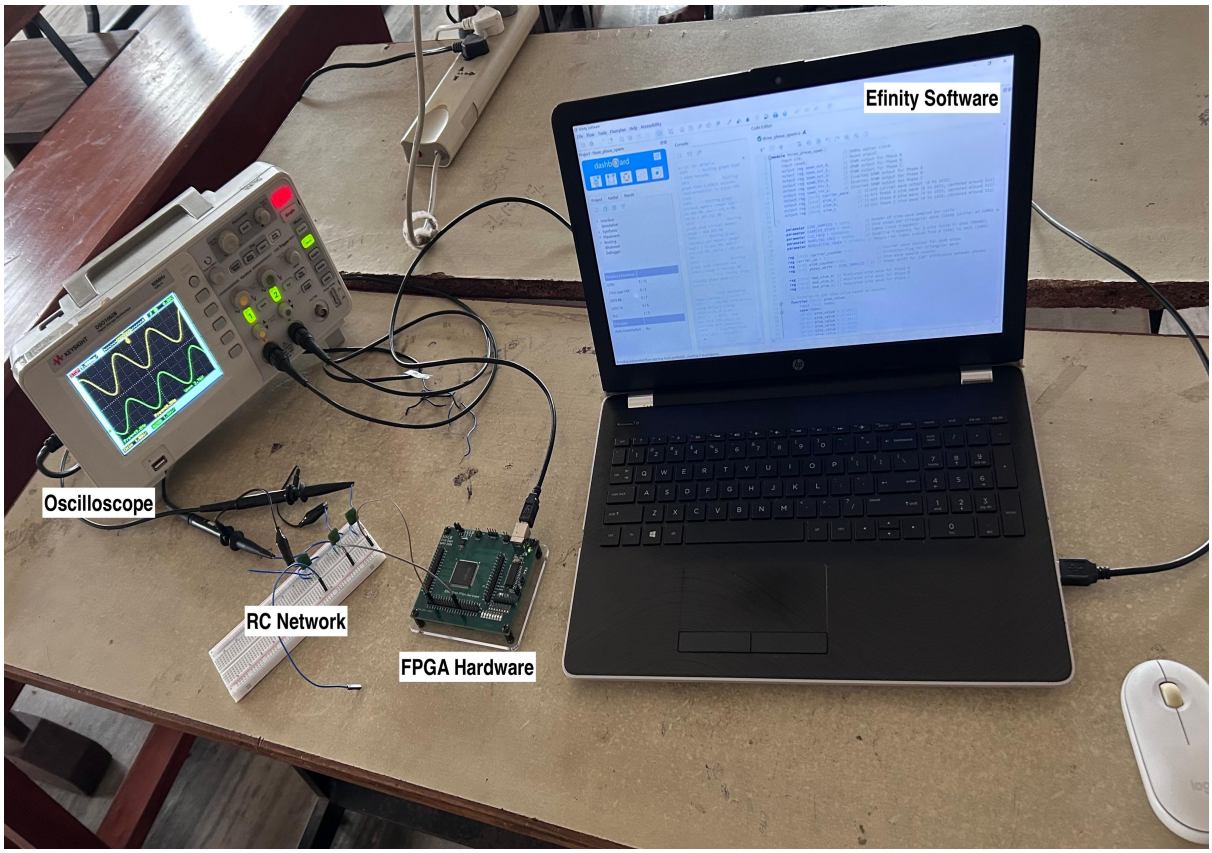


Figure 5.9: Three phase hardware setup

and B. Both waveforms are sinusoidal and 120 ° out of phase, adhering to the standard three-phase power system convention. The output frequency is approximately 48.5 Hz, as indicated on the display, which confirms proper SPWM signal generation and filtering. Similarly, this oscilloscope screenshot shows the waveforms for phases A and C. These are also sinusoidal

and 120 ° apart, ensuring that the phase shift between A, B, and C is consistent. The frequency is nearly 49 Hz, highlighting stable waveform generation and minimal deviation in output.

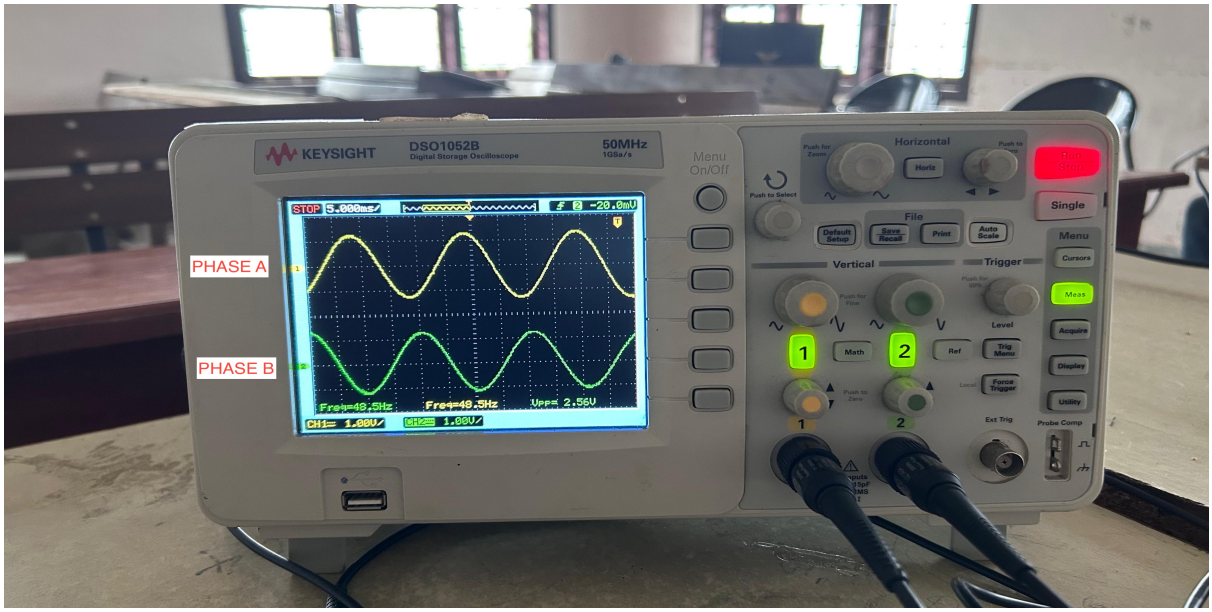


Figure 5.10: Phase A and Phase B in digital oscilloscope

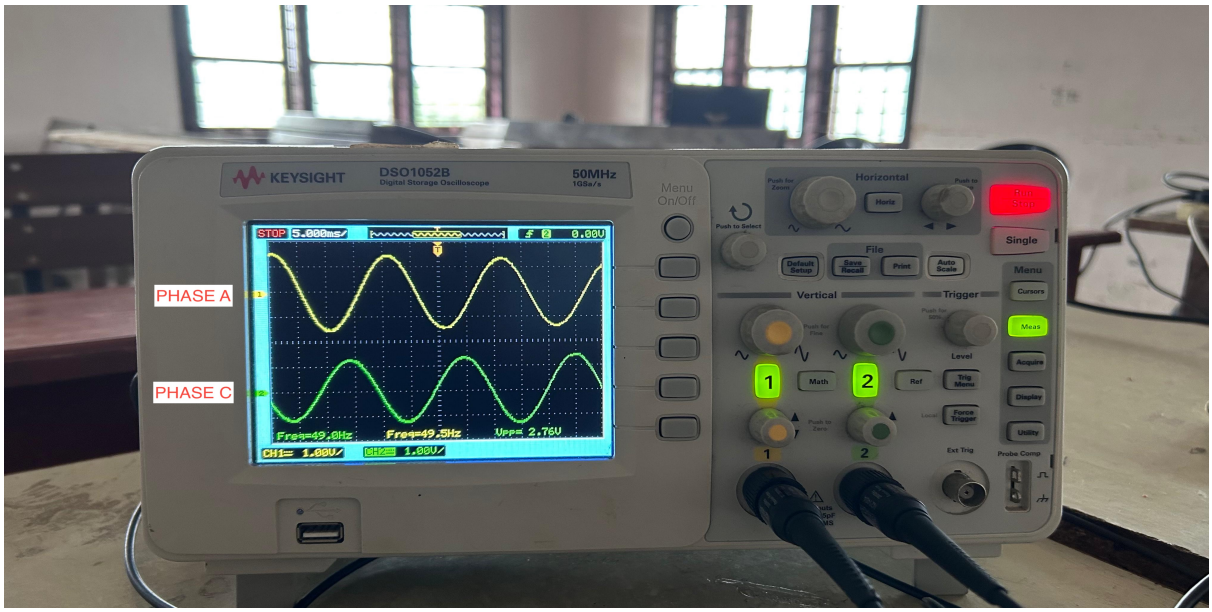


Figure 5.11: Phase A and Phase C obtained in digital oscilloscope

6 CONCLUSION

This dissertation has successfully designed and implemented an innovative FPGA-based controller card for three-phase inverter systems, demonstrating significant advancements in power electronics control technology. The comprehensive approach encompassed both theoretical design and practical implementation, resulting in a robust solution for modern inverter applications.

The FPGA-based controller uses Sinusoidal Pulse Width Modulation (SPWM) techniques to generate high-quality three-phase sinusoidal waveforms with minimal harmonic distortion. Implementation on the T20Q144I4 FPGA platform has proven to be effective, providing the necessary processing power and flexibility for real-time control adjustments. Hardware validation through both simulation and practical testing confirms the viability of the proposed design.

The PCB design represents a sophisticated integration of power electronics principles, incorporating careful consideration of component placement, signal integrity, thermal management, and EMI/EMC concerns. The four-layer design with dedicated ground and power planes provides an excellent balance of performance and manufacturability. The clear separation between the power and control sections ensures reliable operation in noisy electrical environments.

The control system architecture, based on synchronous reference frame theory with PI controllers, demonstrates excellent performance in voltage and current regulation. The dual-loop control structure provides a fast dynamic response and robust operation under varying load conditions. The implementation of coordinate transformations simplifies the control problem by converting time-varying AC quantities into DC-like quantities in a rotating reference frame.

The experimental results validate the theoretical design, showing stable three-phase output with minimal distortion across different operating frequencies. The controller successfully maintains voltage regulation with negligible error, even under challenging load conditions. The hardware implementation confirms the practical feasibility of the design for real-world applications.

This project contributes to the advancement of power electronics control by demonstrating how FPGA technology can be used effectively to create flexible high-performance inverter systems. The modular approach allows for future enhancements, including advanced harmonic management techniques and adaptive control algorithms. The comprehensive documentation of design considerations, component selection parameters, and implementation details provides

valuable information for future research and development in this field.

As power electronics continues to play an increasingly critical role in renewable energy systems, electric vehicles, and industrial applications, this FPGA-based controller offers a promising solution that combines performance, flexibility, and reliability in a cost-effective package.

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A Appendix A: Sine Look Up Table Code

The following is the Verilog code for the sine lookup table:

```
module sine_lut (
    input [9:0] index,          // 10-bit input for index
    output reg [10:0] sine      // 11-bit sine wave output
);
    always @(*) begin
        case (index)
            10'd0: sine_value = 11'd512;
            10'd1: sine_value = 11'd515;
            10'd2: sine_value = 11'd518;
            10'd3: sine_value = 11'd521;
            10'd4: sine_value = 11'd524;
            10'd5: sine_value = 11'd527;
            10'd6: sine_value = 11'd530;
            10'd7: sine_value = 11'd533;
            :                          :
            :                          :
            :                          :
            :                          :
            :                          :
            //1024 sine samples
            10'd1021: sine_value = 11'd502;
            10'd1022: sine_value = 11'd505;
            10'd1023: sine_value = 11'd508;
            default: sine = 11'd512;
        endcase
    end
endmodule
```

Listing 1: Sine Lookup Table (LUT) Code

B Appendix B: Sine Wave Generator Code

The following is the Verilog code for the sine Wave Generator:

```
`include "sine_lut.v"
module sine_wave_gen (
    input clk,                  // Clock signal
    input reset,                // Reset signal
    input [9:0] samples,        // Number of samples per sine wave cycle
    output reg [10:0] sine_a,   // Phase A sine value
    output reg [10:0] sine_b,   // Phase B sine value
    output reg [10:0] sine_c    // Phase C sine value
);
    reg [9:0] counter = 0;              // Counter for sine LUT index
    wire [10:0] lut_value_a, lut_value_b, lut_value_c;
    wire [9:0] phase_shift = samples / 3; // 120-degree phase shift

    sine_lut lut_a (.index(counter), .sine(lut_value_a));
    sine_lut lut_b (.index((counter + phase_shift) % samples),
       .sine(lut_value_b));
    sine_lut lut_c (.index((counter + 2 * phase_shift) % samples),
       .sine(lut_value_c));

    always @(posedge clk or posedge reset) begin
        if (reset) begin
            counter <= 0;
        end else begin
            if (counter < samples - 1)
                counter <= counter + 1;
            else
                counter <= 0;

            sine_a <= lut_value_a;
            sine_b <= lut_value_b;
            sine_c <= lut_value_c;
        end
    end
endmodule
```

Listing 2: Sine Wave Generator Code

C Appendix C: Carrier Wave Generator

The following is the Verilog code for the Carrier Wave Generator:

```
module carrier_wave_gen (
    input clk,                  // Clock signal
    input reset,                // Reset signal
    output reg [10:0] carrier   // Carrier wave output
);
    parameter MODULUS = 1250;   // Modulus for 20 kHz triangular wave

    reg direction = 1;          // Direction of carrier: 1 = up, 0 =
        down
    reg [10:0] counter = 0;

    always @(posedge clk or posedge reset) begin
        if (reset) begin
            counter <= 0;
            direction <= 1;
        end else begin
            if (direction) begin
                if (counter < MODULUS - 1)
                    counter <= counter + 1;
                else
                    direction <= 0; // Switch to decrementing
            end else begin
                if (counter > 0)
                    counter <= counter - 1;
                else
                    direction <= 1; // Switch to incrementing
            end
            carrier <= counter;
        end
    end
endmodule
```

Listing 3: Carrier Wave Generator

D Appendix D: Single Phase SPWM Generator

The following is the Verilog code for the Single Phase SPWM Generator:

```
`include "sine_wave_gen.v"
`include "carrier_wave_gen.v"

module spwm_top (
    input clk,                  // 50MHz master clock
    input reset,                // Reset signal
    output spwm_out,            // SPWM output
    output spwm_inv,            // Inverted SPWM output
    output [10:0] carrier_wave, // Carrier wave output
    output [10:0] sine_wave     // Sine wave output
);
    parameter SINE_SAMPLES = 1024;       // Samples per sine wave cycle
    parameter MODULATION_INDEX = 10'd973; // Modulation index (50% to
        100%)

    wire [10:0] mod_sine; // Modulated sine wave

    // Instantiate Sine Wave Generator
    sine_wave_gen sine_gen (
        .clk(clk),
        .reset(reset),
        .samples(SINE_SAMPLES),
        .sine_a(sine_wave), // Single sine wave output
        .sine_b(),          // Unused outputs
        .sine_c()
    );

    // Instantiate Carrier Wave Generator
    carrier_wave_gen carrier_gen (
        .clk(clk),
        .reset(reset),
        .carrier(carrier_wave)
    );

    // Apply modulation index scaling
    assign mod_sine = 512 + ((sine_wave - 512) * MODULATION_INDEX) >>
```

```
        10;

    // Generate SPWM outputs
    assign spwm_out = (mod_sine > carrier_wave) ? 1 : 0;
    assign spwm_inv = ~spwm_out;

endmodule
```

Listing 4: Single Phase SPWM Generator

E Appendix E: Three Phase SPWM Generator

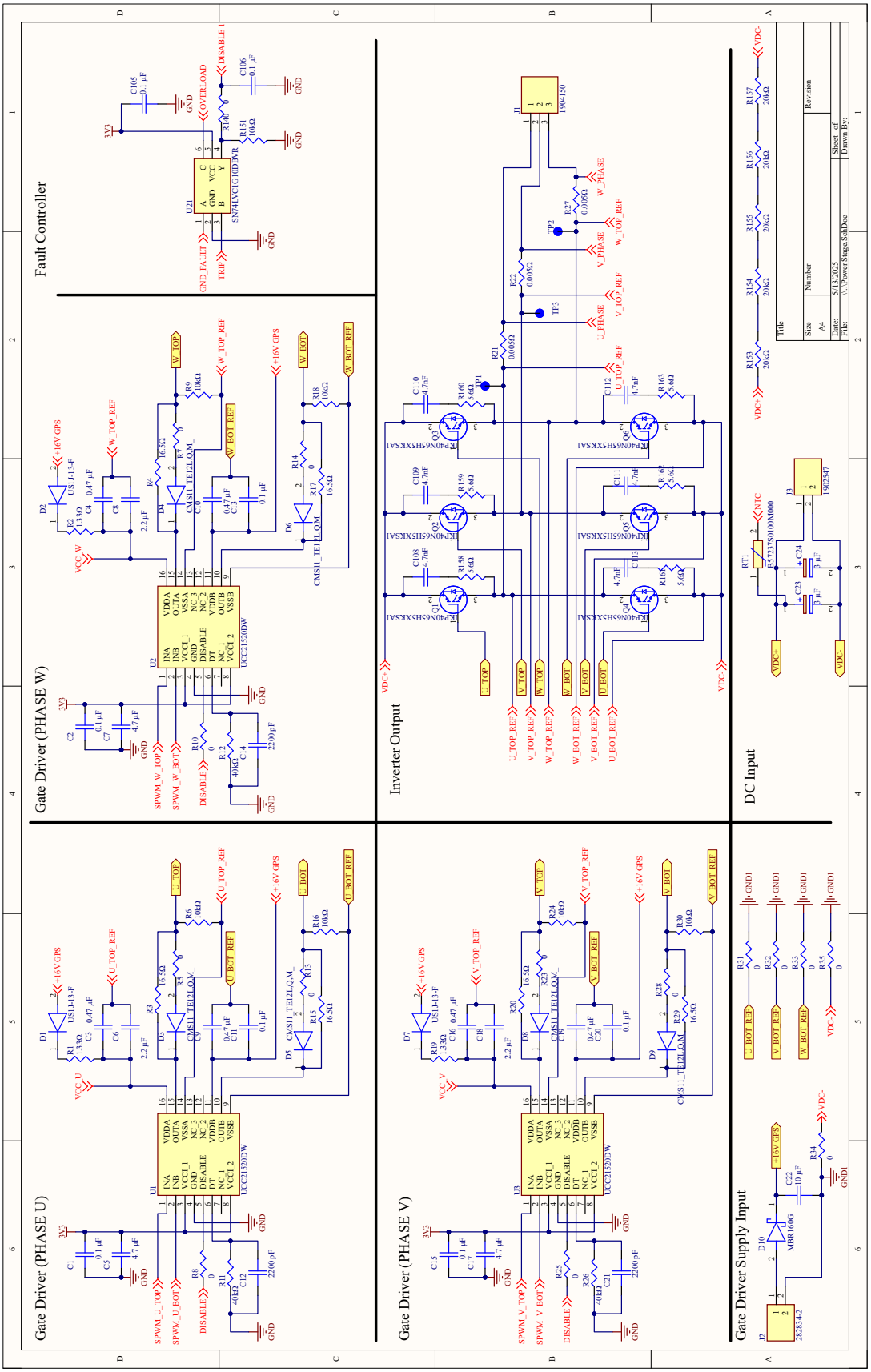
The following is the Verilog code for the Three Phase SPWM Generator:

```
`include "sine_wave_gen.v"
`include "carrier_wave_gen.v"
module spwm_top (
    input clk,                  // 50MHz master clock
    input reset,                // Reset signal
    output spwm_out_0,          // SPWM output for Phase A
    output spwm_out_1,          // SPWM output for Phase B
    output spwm_out_2,          // SPWM output for Phase C
    output spwm_inv_0,          // Inverted SPWM output for Phase A
    output spwm_inv_1,          // Inverted SPWM output for Phase B
    output spwm_inv_2,          // Inverted SPWM output for Phase C
    output [10:0] carrier_wave, // Carrier wave output
    output [10:0] sine_a,       // Phase A sine wave
    output [10:0] sine_b,       // Phase B sine wave
    output [10:0] sine_c        // Phase C sine wave
);
    parameter SINE_SAMPLES = 1024;   // Samples per sine wave cycle
    parameter MODULATION_INDEX = 10'd973; // Modulation index (50% to
        100%)

    wire [10:0] mod_sine_a, mod_sine_b, mod_sine_c;

    // Instantiate Sine Wave Generator
    sine_wave_gen sine_gen (
        .clk(clk),
        .reset(reset),
        .samples(SINE_SAMPLES),
        .sine_a(sine_a),
        .sine_b(sine_b),
        .sine_c(sine_c)
    );

    // Instantiate Carrier Wave Generator
    carrier_wave_gen carrier_gen (
        .clk(clk),
        .reset(reset),
```

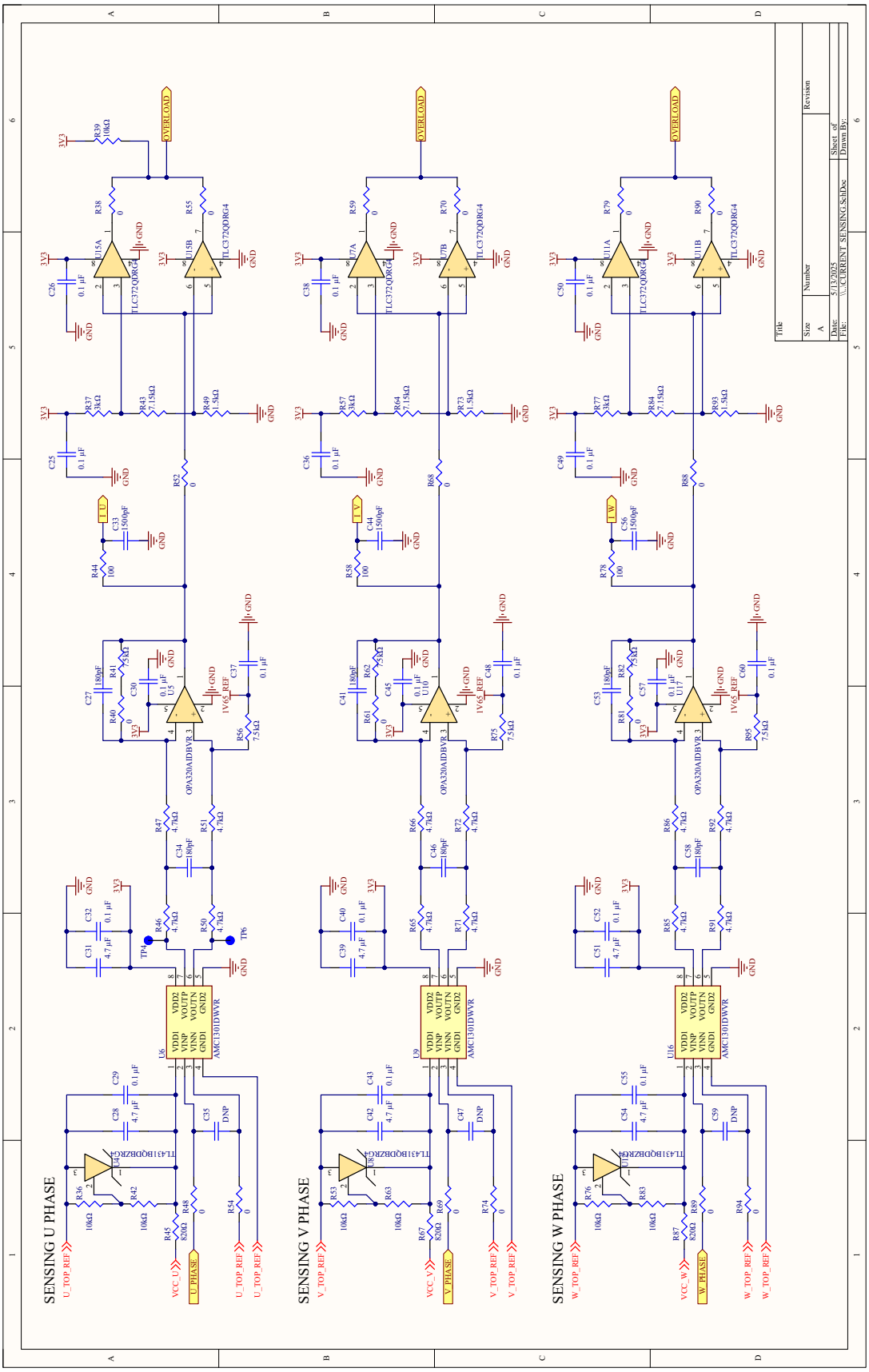
```
        .carrier(carrier_wave)
    );

    // Apply modulation index scaling
    assign mod_sine_a = 512 + ((sine_a - 512) * MODULATION_INDEX) >>
        10;
    assign mod_sine_b = 512 + ((sine_b - 512) * MODULATION_INDEX) >>
        10;
    assign mod_sine_c = 512 + ((sine_c - 512) * MODULATION_INDEX) >>
        10;

    // Generate SPWM outputs
    assign spwm_out_0 = (mod_sine_a > carrier_wave) ? 1 : 0;
    assign spwm_inv_0 = ~spwm_out_0;

    assign spwm_out_1 = (mod_sine_b > carrier_wave) ? 1 : 0;
    assign spwm_inv_1 = ~spwm_out_1;

    assign spwm_out_2 = (mod_sine_c > carrier_wave) ? 1 : 0;
    assign spwm_inv_2 = ~spwm_out_2;
endmodule
```

Listing 5: Three Phase SPWM Generator Code

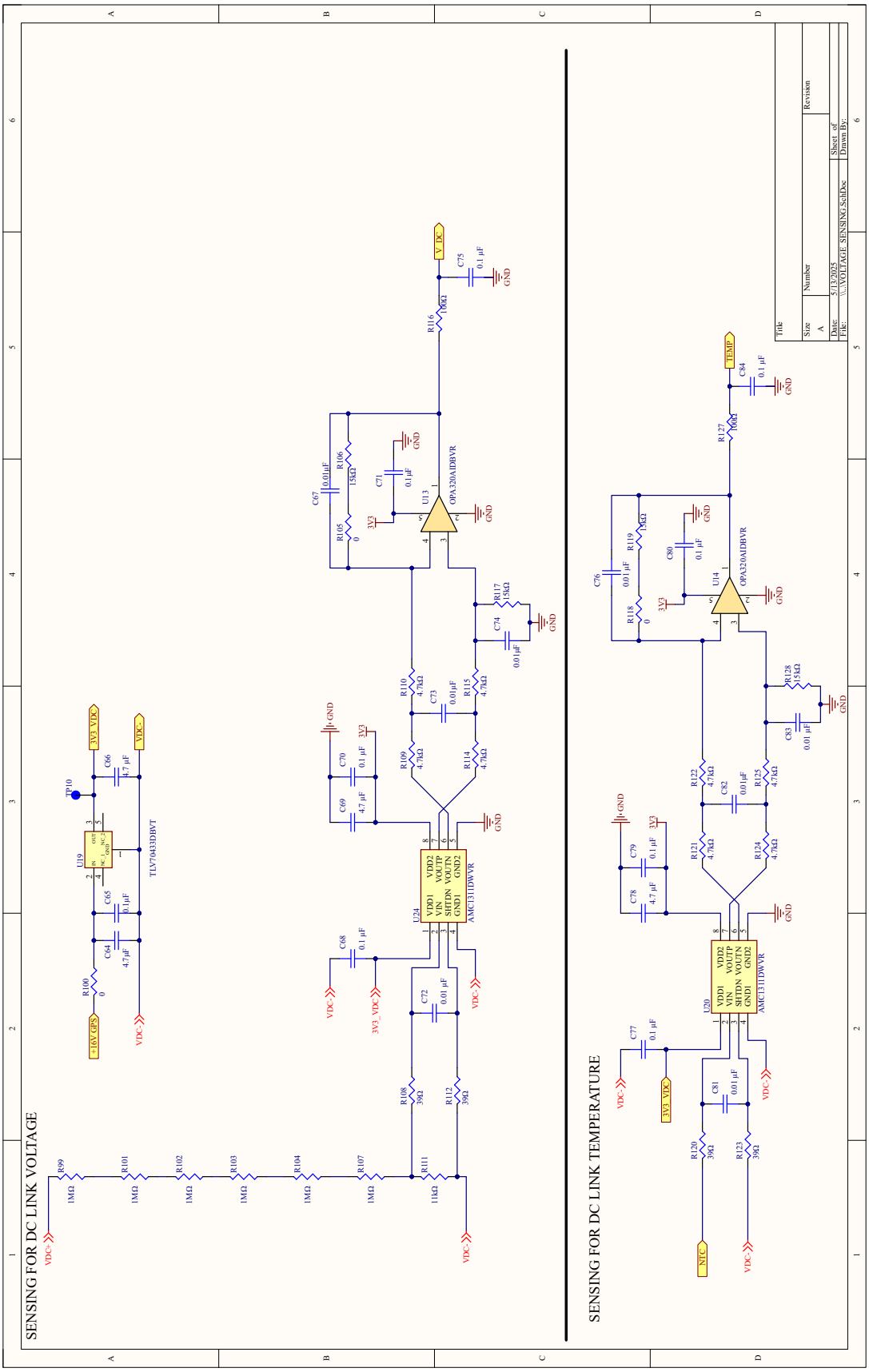
Appendix F: Power Stage



Appendix G: Current Sensing



Appendix H: Voltage Sensing



Appendix I: Pin Configuration